DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.E. VLSI DESIGN

Regulation 2019



CHOICE BASED CREDIT SYSTEM

(I - IV SEMESTERS CURRICULUM & SYLLABUS)



Sri Eshwar College of Engineering

(An Autonomous Institution) (Approved by AICTE, Affiliated to Anna University, Chennai) Kondampatti (Post), Kinathukadavu, Coimbatore - 641202.

M.E. VLSI Design

Regulation 2019

Semester I

| SI.No. | Course Code | Course Title | Category | Contact Periods | L | т | Ρ | С |
|--------|----------------|--|----------|--------------------|----|---|---|----|
| THEORY | (| | | | | | | |
| 1 | P19MA103 | Applied Mathematics for Electronics Engineers | FC | 4 | 3 | 1 | 0 | 4 |
| 2 | P19VL101 | Advanced Digital System Design | PC | 3 | 3 | 0 | 0 | 3 |
| 3 | P19VL102 | CMOS Digital VLSI Design | PC | 3 | 3 | 0 | 0 | 3 |
| 4 | P19VL3XX | Program Elective I | PE | 3 | 3 | 0 | 0 | 3 |
| 5 | P19VL3XX | Program Elective II | PE | 3 | 3 | 0 | 0 | 3 |
| 6 | P19ED102 | Research Methodology and IPR | MC | 3 | 3 | 0 | 0 | 3 |
| PRACTI | CALS | | | | | | | |
| 7 | P19VL111 | VLSI Design Laboratory I | PC | 4 | 0 | 0 | 4 | 2 |
| 8 | P19AC5XX | Audit Course I | AC | 2 | 2 | 0 | 0 | NC |
| | | TOTAL | | 25 | 20 | 1 | 4 | 21 |

Semester II

| | | Semes | ter II | | | | | |
|---------|----------------|---------------------------|----------|--------------------|----|---|---|----|
| SI.No. | Course Code | Course Title | Category | Contact Periods | L | т | Р | С |
| THEORY | | | | | | | | |
| 1 | P19VL104 | Analog IC Design | PC | 4 | 3 | 1 | 0 | 4 |
| 2 | P19VL105 | Low Power VLSI Design | PC | 3 | 3 | 0 | 0 | 3 |
| 3 | P19VL106 | Testing of VLSI Circuits | PC | 3 | 3 | 0 | 0 | 3 |
| 4 | P19VL3XX | Program Elective III | PE | 3 | 3 | 0 | 0 | 3 |
| 5 | P19VL3XX | Program Elective IV | PE | 3 | 3 | 0 | 0 | 3 |
| PRACTIC | ALS | | | | | | | |
| 6 | P19VL112 | VLSI Design Laboratory II | PC | 4 | 0 | 0 | 4 | 2 |
| 7 | P19VL201 | Mini Project | PW | 4 | 0 | 0 | 4 | 2 |
| 8 | P19AC5XX | Audit Course II | AC | 2 | 2 | 0 | 0 | NC |
| | | TOTAL | | 26 | 17 | 1 | 8 | 20 |

Semester III

| SI.No. | Course Code | Course Title | Category | Contact Periods | L | т | Ρ | С |
|--------|----------------|----------------------|----------|--------------------|---|---|----|----|
| THEORY | ſ | | | | | | | |
| 1 | P19VL3XX | Program Elective V | PE | 3 | 3 | 0 | 0 | 3 |
| 2 | P19OE4XX | Open Elective | OE | 3 | 3 | 0 | 0 | 3 |
| PRACTI | CALS | | | | | | | |
| 3 | P19VL202 | Project Work Phase I | PW | 16 | 0 | 0 | 16 | 8 |
| | | TOTAL | | 22 | 6 | 0 | 16 | 14 |

Semester IV

| SI.No. | Course Code | 1 | Course Title | 6 Eve | Category | Contact Periods | L | т | Ρ | С |
|--------|----------------|------------|-----------------|---------------|----------|--------------------|---|---|----|----|
| PRACTI | CALS | | seuderamp | COL BALLYS CO | 61161146 | | | | | |
| 1 | P19VL203 | Project Wo | rk Phase II | | PW | 32 | 0 | 0 | 32 | 16 |
| | | | TOTAL | A | | 32 | 0 | 0 | 32 | 16 |

TOTAL NO. OF CREDITS: 70

SUMMARY

| SI No | Course | Cr | edits pe | r semest | ter | Cradita | Credit 0/ |
|--------|----------|--------------|--------------|----------|-----|---------|-----------|
| 51.NO. | Category | I | II | III | IV | Credits | |
| 1 | FC | 4 | - | - | - | 4 | 5.7 |
| 2 | PC | 8 | 12 | - | - | 20 | 28.5 |
| 3 | PE | 6 | 6 | 3 | - | 15 | 21.2 |
| 4 | OE | Ĺ | - | 3 | - | 3 | 4.2 |
| 5 | PW | 1 | 2 | 8 | 16 | 26 | 37.1 |
| 6 | мс | 2 | - | - - | - | 2 | 2.8 |
| 7 | AC | \checkmark | \checkmark | - | - | - | _ |
| Total | | 20 | 20 | 14 | 16 | 70 | 100 |

| SI.No | Course Code | Subject | Course Category | L | т | Ρ | С |
|-------|----------------|---|--------------------|---|---|---|---|
| 1 | P19MA103 | Applied Mathematics for Electronics Engineers | FC | 3 | 1 | 0 | 4 |

FOUNDATION COURSE (FC)

PROGRAM CORES (PC)

| SI.No | Course Code | Subject | Course Category | L | т | Ρ | С |
|-------|----------------|--------------------------------|--------------------|---|---|---|---|
| 1 | P19VL101 | Advanced Digital System Design | PC | 3 | 0 | 0 | 3 |
| 2 | P19VL102 | CMOS Digital VLSI Design | PC | 3 | 0 | 0 | 3 |
| 3 | P19VL111 | VLSI Design Laboratory I | PC | 3 | 0 | 0 | 3 |
| 4 | P19VL104 | Analog IC Design | PC | 4 | 0 | 0 | 4 |
| 5 | P19VL105 | Low Power VLSI Design | PC | 3 | 0 | 0 | 3 |
| 6 | P19VL106 | Testing of VLSI Circuits | PC | 3 | 0 | 0 | 3 |
| 7 | P19VL112 | VLSI Design Laboratory II | PC | 3 | 0 | 0 | 3 |

PROGRAM ELECTIVES (PE)

| SI.No | Course Code | Subject | Course Category | L | т | Ρ | С |
|-------|----------------|--|--------------------|---|---|---|---|
| | | SEMESTER I – ELECTIVE I | | | | | |
| 1 | P19VL301 | Device Modeling | PE | 3 | 0 | 0 | 3 |
| 2 | P19VL302 | RF IC Design | PE | 3 | 0 | 0 | 3 |
| 3 | P19VL303 | Design of Analog Filters and Signal Conditioning Circuits | PE | 3 | 0 | 0 | 3 |
| 4 | P19VL304 | CAD for VLSI Circuits | PE | 3 | 0 | 0 | 3 |
| | | SEMESTER I – ELECTIVE II | | | | | |
| 5 | P19VL305 | Embedded System Design | PE | 3 | 0 | 0 | 3 |
| 6 | P19VL306 | Advanced Microprocessors and Architectures | PE | 3 | 0 | 0 | 3 |
| 7 | P19VL307 | DSP Processor Architecture and Programming | PE | 3 | 0 | 0 | 3 |
| 8 | P19VL308 | Digital Control Engineering | PE | 3 | 0 | 0 | 3 |
| | | SEMESTER II - ELECTIVE III | | | | | |
| 9 | P19VL309 | DSP Integrated Circuits | PE | 3 | 0 | 0 | 3 |
| 10 | P19VL310 | VLSI Signal Processing | PE | 3 | 0 | 0 | 3 |
| 11 | P19VL311 | Soft Computing and Optimization Techniques | PE | 3 | 0 | 0 | 3 |
| 12 | P19VL312 | Reconfigurable Architectures | PE | 3 | 0 | 0 | 3 |
| | | SEMESTER II – ELECTIVE IV | | | | | |
| 13 | P19VL313 | CMOS Digital VLSI Design | PE | 3 | 0 | 0 | 3 |
| 14 | P19VL314 | Networks on Chip | PE | 3 | 0 | 0 | 3 |
| 15 | P19VL315 | Design and Analysis of Computer Algorithms | PE | 3 | 0 | 0 | 3 |
| 16 | P19VL316 | Digital Image Processing | PE | 3 | 0 | 0 | 3 |
| | | SEMESTER III – ELECTIVE V | | | | | |
| 17 | P19VL317 | MEMS and NEMS | PE | 3 | 0 | 0 | 3 |
| 18 | P19VL318 | Signal Integrity for High Speed Design | PE | 3 | 0 | 0 | 3 |
| 19 | P19VL319 | Nanoscale Devices | PE | 3 | 0 | 0 | 3 |
| 20 | P19VL320 | Scripting Languages for VLSI | PE | 3 | 0 | 0 | 3 |

OPEN ELECTIVES (OE)

| SI. No | Course Code | Subject | Course Category | L | т | Ρ | с |
|--------|----------------|---------------------|--------------------|---|---|---|---|
| 1 | P190E401 | Business Analytics | OE | 3 | 0 | 0 | 3 |
| 2 | P190E402 | Industrial Safety | OE | 3 | 0 | 0 | 3 |
| 3 | P190E403 | Operations Research | OE | 3 | 0 | 0 | 3 |
| 5 | P190E404 | Composite Materials | OE | 3 | 0 | 0 | 3 |

PROJECT WORK (PW)

| SI. No | Course Code | Subject | Course Category | L | т | Ρ | с |
|--------|----------------|-----------------------|--------------------|---|---|----|----|
| 1 | P19VL201 | Mini Project | PW | 0 | 0 | 4 | 2 |
| 2 | P19VL202 | Project Work Phase I | PW | 0 | 0 | 16 | 8 |
| 3 | P19VL203 | Project Work Phase II | PW | 0 | 0 | 32 | 16 |

MANDATORY COURSE (MC)

| SI. No | Course Code | Leadership & Subject | Excellence | Course Category | L | т | Р | с |
|-----------|----------------|------------------------------|------------|--------------------|---|---|---|---|
| 1 | P19ED102 | Research Methodology and IPR | Α. | MC | 2 | 0 | 0 | 2 |

AUDIT COURSES (AC)

| Course Code | Subject | Course Category | L | т | Ρ | С |
|----------------|--|--|--|---|--|---|
| P19AC501 | English for research paper writing | AC | 2 | 0 | 0 | NC |
| P19AC502 | Disaster Management | AC | 2 | 0 | 0 | NC |
| P19AC503 | Sanskrit for Technical Knowledge | AC | 2 | 0 | 0 | NC |
| P19AC504 | Value Education | AC | 2 | 0 | 0 | NC |
| P19AC505 | Constitution of India | AC | 2 | 0 | 0 | NC |
| P19AC506 | Pedagogy Studies | AC | 2 | 0 | 0 | NC |
| P19AC507 | Stress Management by Yoga | AC | 2 | 0 | 0 | NC |
| P19AC508 | Personality Development through Life Enlightenment Skills. | AC | 2 | 0 | 0 | NC |
| | Code P19AC501 P19AC502 P19AC503 P19AC504 P19AC505 P19AC506 P19AC507 P19AC508 | CodeSubjectP19AC501English for research paper writingP19AC502Disaster ManagementP19AC503Sanskrit for Technical KnowledgeP19AC504Value EducationP19AC505Constitution of IndiaP19AC506Pedagogy StudiesP19AC507Stress Management by YogaP19AC508Personality Development through Life Enlightenment Skills. | CodeSubjectCategoryP19AC501English for research paper writingACP19AC502Disaster ManagementACP19AC503Sanskrit for Technical KnowledgeACP19AC504Value EducationACP19AC505Constitution of IndiaACP19AC506Pedagogy StudiesACP19AC507Stress Management by YogaACP19AC508Personality Development through Life Enlightenment Skills.AC | CodeSubjectCategoryLP19AC501English for research paper writingAC2P19AC502Disaster ManagementAC2P19AC503Sanskrit for Technical KnowledgeAC2P19AC504Value EducationAC2P19AC505Constitution of IndiaAC2P19AC506Pedagogy StudiesAC2P19AC507Stress Management by YogaAC2P19AC508Personality Development through Life Enlightenment Skills.AC2 | CodeSubjectCategoryLTP19AC501English for research paper writingAC20P19AC502Disaster ManagementAC20P19AC503Sanskrit for Technical KnowledgeAC20P19AC504Value EducationAC20P19AC505Constitution of IndiaAC20P19AC506Pedagogy StudiesAC20P19AC507Stress Management by YogaAC20P19AC508Personality Development through Life Enlightenment Skills.AC20 | CodeSubjectCategoryLTPP19AC501English for research paper writingAC200P19AC502Disaster ManagementAC200P19AC503Sanskrit for Technical KnowledgeAC200P19AC504Value EducationAC200P19AC505Constitution of IndiaAC200P19AC506Pedagogy StudiesAC200P19AC507Stress Management by YogaAC200P19AC508Personality Development through Life Enlightenment Skills.AC200 |

M.E. VLSI Design

Regulation 2019

Semester I

| SI.No. | Course Code | Course Title | Category | Contact Periods | L | т | Ρ | С |
|--------|----------------|--|----------|--------------------|----|---|---|----|
| THEORY | 1 | | | | | | | |
| 1 | P19MA103 | Applied Mathematics for Electronics Engineers | FC | 4 | 3 | 1 | 0 | 4 |
| 2 | P19VL101 | Advanced Digital System Design | PC | 3 | 3 | 0 | 0 | 3 |
| 3 | P19VL102 | CMOS Digital VLSI Design | PC | 3 | 3 | 0 | 0 | 3 |
| 4 | P19VL3XX | Program Elective I | PE | 3 | 3 | 0 | 0 | 3 |
| 5 | P19VL3XX | Program Elective II | PE | 3 | 3 | 0 | 0 | 3 |
| 6 | P19ED102 | Research Methodology and IPR | MC | 3 | 3 | 0 | 0 | 3 |
| PRACTI | CALS | | | | | | | |
| 7 | P19VL111 | VLSI Design Laboratory I | PC | 4 | 0 | 0 | 4 | 2 |
| 8 | P19AC5XX | Audit Course I | AC | 2 | 2 | 0 | 0 | NC |
| | | TOTAL | | 26 | 20 | 1 | 4 | 21 |



| D10 | MA 102 | APPL | IED MATHEMATICS FOR COMMUNICATION | L | т | Ρ | C | |
|---------------|---|-------------------------------|--|------------|-----------|---------|-------------|--|
| PI9MAIU3 | | ENGINEERING 3 1 | | | | | 4 | |
| | | Δfter | completion of this course, students will be able to | | | | | |
| | | CO1 | (Apply) Apply the concepts of fuzzy sets, knowled | lge repr | esentati | on | К3 | |
| Outc | omes | CO2 | (Apply) Apply different techniques in matrix theor | ry to sol | ve linea | ar | К3 | |
| oute | CO3 (Analyze) Test the nature of linear transformations and analyze the | | | | | | | |
| | | CO4 | (Apply) Apply the principles of optimality, | formulat | ion an | d | К3 | |
| | | CO5 | (Analyze) Examine the basic concepts of queuing the skills in various queuing models | neory an | d acquir | re | K4 | |
| | | | skiis in valious queunig models. | | | | | |
| MOD | ULE I | FUZZ | Y LOGIC | | | | 12 | |
| Class | ical logic | – Multi | -valued logics – Fuzzy propositions – Fuzzy quantifiers | | | | | |
| | j | | | | | | | |
| MOD | ULE II | MATE | RIX THEORY | | | | 12 | |
| Chole meth | esky deco od - Sing | mposit ular va | ion - Generalized eigenvectors - Canonical basis - QR lue decomposition. | t factoriz | zation - | Least | squai | |
| | | | | | | | | |
| MOD | | | AR PROGRAMMING | | thad | Dual | 12 | |
| meth | od. | n inea | r programming problem – Graphical solution – Sim | piex me | ethod – | Duai | simp | |
| MOD | ULE IV | DYN | | | | | 12 | |
| Dyna dynai | mic prog mic progr | rammir ammin | ng – Principle of optimality – Forward and backwar g – Problem of dimensionality. | d recurs | sion – A | Applica | tions | |
| | | | | | | | | |
| Mark | ovian mo | dels – | Birth and death process. Steady state results: Single | e and m | ultiple s | erver | 12 queui | |
| moae | eis - Littie | e s form | iuia. | | Cotal: 6 | 0 Hou | irs | |
| техт | BOOKS | | | | | ••• | | |
| 1 | Taha H. Delhi, 2 | A., "O 016. | perations Research: An Introduction", 9 th Edition, Pea | arson Ed | lucation | , Asia, | New | |
| 2 | Bronson | R "M | atrix Operations" Schaum's Outline Series 2 nd Edition | n McGr | aw Hill | 2011 | | |
| 3 | George of India | J. Klir a Pvt. Lt | and Yuan, B., "Fuzzy sets and Fuzzy logic, Theory and d., 1997. | Applicat | ions", P | rentice | : Hall | |
| REFE | RENCES | : | | | | | | |
| 1 | Johnson Enginee | R. A. rs", 8 th | , Miller, I and Freund J., "Miller and Freund's Pro Edition, Pearson Education, Asia, 2015. | bability | and St | atistic | s for | |
| 2 | Gross D 4 th Editi | on, Joh | tle J. F., Thompson J. M and Harris C. M., "Fundame n Wiley, 2014. | entals of | Queuir | ng The | ory", | |

| D10VI 101 | ADVANCED DIGITAL SYSTEM DESIGN | | | Т | Р | С | | | |
|--|--------------------------------|---|---|---------------|---|--------------------|--|--|--|
| FIJVLIUI | | ADVANCED DIGITAL SYSTEM DESIGN 3 0 | | | | | | | |
| | | | | | | | | | |
| | Upon | completion of this course, students will be able to | | | | | | | |
| | CO1 | (Apply) Design sequential circuit design. | | | | K3 | | | |
| | CO2 | (Analyze) Analyze sequential digital circuits. | | | | K4 | | | |
| Outcomes | CO3 | (Analyze) Analyze the fault diagnosis algorithms an schemes. | Ilyze) Analyze the fault diagnosis algorithms and test generation mes. | | | | | | |
| | C04 | CO4 (Analyze) Analyze sequential circuits and design synchronous design using programmable devices. | | | | | | | |
| | CO5 | (Apply) Design digital circuits utilizing various construct | s of Ver | ilog . | | K3 | | | |
| | | | | | | | | | |
| MODULE I | SEQU | JENTIAL CIRCUIT DESIGN | | | | 9 | | | |
| Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, st assignment and reduction-Design of synchronous sequential circuits design of iterative circuits-A and realization using ASM | | | | | | e table 1 chart | | | |
| | VCAN | CHRONOUS SEQUENTIAL CIRCUIT DESIGN | | | | 0 | | | |

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

MODULE III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS

Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test

MODULE IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000

MODULE V SYSTEM DESIGN USING VERILOG

Hardware Modeling with Verilog HDL – Logic System, Data Types and Operators For Modeling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machinesstructural modeling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier-Divider – Design of simple microprocessor

Total : 45 HOURS

9

9

9

REFERENCES:

- Charles H.Roth Jr "Fundamentals of Logic Design" Thomson Learning 2004
- M.D.Ciletti, Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999
- M.G.Arnold, Verilog Digital Computer Design, Prentice Hall (PTR), 1999.
- Nripendra N Biswas "Logic Design Theory" Prentice Hall of India, 2001
- Parag K.Lala "Fault Tolerant and Fault Testable Hardware Design" B S

Publications,2002

- Parag K.Lala "Digital system Design using PLD" B S Publications, 2003
- S. Palnitkar , Verilog HDL A Guide to Digital Design and Synthesis, Pearson , 2003.

| D10// 102 | CMOS DIGITAL VEST DESIGN | | | | Р | С | |
|-----------|--------------------------|--|--|--|---|----|--|
| PISVLIUZ | CHOS | 3 0 0 | | | | | |
| | | | | | | | |
| | Upon o | completion of this course, students will be able to | | | | | |
| | CO1 | 01 (Analyze) Analyze the performance of CMOS Inverter circuit. | | | | | |
| Outcomos | CO2 | (Apply) Design Combinational logic circuits. | | | | K3 | |
| Outcomes | CO3 | (Apply) Design Sequential logic circuits. | | | | K3 | |
| | CO4 | 4 (Apply) Discuss design methodology of arithmetic building block. | | | | | |
| | CO5 | CO5 (Understand) Understand various interconnect and clocking strategies | | | | | |
| | | | | | | | |

MODULE I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, Technology Scaling - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters.

MODULE II COMBINATIONAL LOGIC CIRCUITS

Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

MODULE III SEQUENTIAL LOGIC CIRCUITS

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pulse and sense amplifier based Registers, Non bistable Sequential Circuits.

MODULE IV ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

MODULE V INTERCONNECT AND CLOCKING STRATEGIES

Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Self-Timed Circuit Design.

Total: 45 HOURS

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- 1.Jan Rabaey, Anantha Chandrakasan, B Nikolic,
Second Edition, Feb 2003, Prentice Hall of India."Digital Integrated Circuits: A Design Perspective".
- 2. Jacob Baker "CMOS: Circuit Design, Layout, and Simulation, Third Edition", Wiley IEEE Press 2010 3rd Edition.
- 3. M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997
- 4. N.Weste, K. Eshraghian, " Principles of CMOS VLSI Design". Second Edition, 1993 Addision Wesley.

| D105D102 | | | | т | Р | С | | |
|----------|--|---|--|---|---|---|--|--|
| PI9ED102 | KESEA | RESEARCH METHODOLOGY AND IPR 3 0 0 | | | | | | |
| | | | | | | | | |
| | Upon c | ompletion of this course, students will be able to | | | | | | |
| | CO1 | O1 (Analyze) Analyze and formulate research problem | | | | | | |
| | CO2 | (Analyze) Carry out research analysis | | | | | | |
| Outcomes | CO3 | 3 (Apply) Follow research ethics | | | | | | |
| | CO4 | (Understand) Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity | | | | | | |
| | CO5 (Understand) Understand about IPR and filing patents in R & D. | | | | | | | |

MODULE I RESEARCH PROBLEM FORMULATION

Meaning of research problem- Sources of research problem, criteria characteristics of a good research problem, errors in selecting a research problem, scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, necessary instrumentations

MODULE II LITERATURE REVIEW

Effective literature studies approaches, analysis, plagiarism, and research ethics.

MODULE III TECHNICAL WRITING / PRESENTATION

Effective technical writing, how to write report, paper, developing a research proposal, format of research proposal, a presentation and assessment by a review committee.

MODULE IV INTRODUCTION TO INTELLECTUAL PROPERTY RIGHTS (IPR)

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

MODULE V INTELLECTUAL PROPERTY RIGHTS (IPR)

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System, IPR of Biological Systems, Computer Software etc.

Traditional knowledge Case Studies, IPR and IITs.

DEFEDENCES.

TOTAL: 45 HOURS

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| REFER | ENCES: |
|-------|--|
| 1 | Asimov, "Introduction to Design", Prentice Hall, 1962. |
| 2 | Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007. |
| 3 | Mayall, "Industrial Design", McGraw Hill, 1992. |
| 4 | Niebel, "Product Design", McGraw Hill, 1974. |
| 5 | Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners" 2010 |
| | |

| P19VL111 | | | I Design Laboratory I | | L | Т | Р | С | | | |
|----------|---|-------------------------------|-----------------------|---|-----------------------------|-----------------------------|------------|-----------|----------|---------|--|
| P19V | | VLSI Desi | 0 0 4 | | | | | 4 | 2 | | |
| | | Upon comp | pletion o | of this course, students will be able to | | | | | | | |
| | | C01 | (Apply design | Apply) Apply the FPGA platform and carry out a series of validations lesign. | | | | | | | |
| | | CO2 | (Apply buildin | pply) Design and carry out time domain simulations of simple analog ilding blocks. | | | | | | | |
| Outco | omes | CO3 | (Apply analog | ply) Design and carry out frequency domain simulations of simple alog building blocks. | | | | | | | |
| | | CO4 | (Anal) circuits | yze) Evaluate the s. | the pole ze | ero behaviors | s of feedb | ack base | ed | K4 | |
| | | CO5 | (Apply | y) Design and con | npute the ir | nput/output i | impedano | ces. | | К3 | |
| | | | | List of E | xperiment | S | | | | | |
| 1. | Unders | standing Syn | nthesis p | rinciples. Back an | notation. | | | | | | |
| 2. | Test v using l | ector genera HDL languag | ation ar Jes. | nd timing analysis | of sequen | ntial and cor | mbinatior | nal logic | design r | ealized | |
| 3. | FPGA r | eal time pro | ogrammi | ng and I/O interfa | cing. | | | | | | |
| 4. | Interfa | cing with Me | emory m | nodules in FPGA Bo | oards. | | | | | | |
| 5. | Verifica | ation of desi | ign funct | ionality implemen | ted in FPGA | <mark>A by capt</mark> urin | g the sig | nal in DS | 60. | | |
| 6. | Real ti | me applicati | ion deve | lopment. | | we | | | | | |
| 7. | Design sequer | Entry Using ntial, concurr | ig VHDL rent stat | or Verilog examp ements and struct | les for Dig tural descri | ital circuit d ption. | escriptio | ns using | HDL lan | guages | |
| | | | | | | | | Total: | 30 HC | URS | |
| REFERE | INCES | | | | | | | | | | |
| 1. | Ming-E | o Lin, Digita | al Syster | n Designs and Pra | ctices using | g Verilog HDI | L and FPG | GAs, Wile | y, 2012. | | |
| 2. | Samir | Palnitkar, Ve | erilog H[| DL, Pearson Educa | tion, 2ndEd | lition, 2004. | | | | | |
| 3. | J.Bhas | kar, A VHDL | Primer, | Prentice Hall, 199 | 98. | | | | | | |
| 4. | M.H.Ra | ashid, Spice | for Circu | uits and Electronic | s using Psp | ice, PHI 199 | 5. | | | | |
| 5. | M.J.S.Smith, Application Specific Integrated Circuits, Pearson Education, 2008. | | | | | | | | | | |

| SI.No | Course Code | Course Title | Course Category | L | т | Ρ | с |
|-------|----------------|--|--------------------|---|---|---|---|
| | | SEMESTER I – ELECTIVE I | | | | | |
| 1 | P19VL301 | Device Modeling | PE | 3 | 0 | 0 | 3 |
| 2 | P19VL302 | RF IC Design | PE | 3 | 0 | 0 | 3 |
| 3 | P19VL303 | Design of Analog Filters and Signal Conditioning Circuits | PE | 3 | 0 | 0 | 3 |
| 4 | P19VL304 | CAD for VLSI Circuits | PE | 3 | 0 | 0 | 3 |
| | | SEMESTER I – ELECTIVE II | | | | | |
| 5 | P19VL305 | Embedded System Design | PE | 3 | 0 | 0 | 3 |
| 6 | P19VL306 | Advanced Microprocessors and Architectures | PE | 3 | 0 | 0 | 3 |
| 7 | P19VL307 | DSP Processor Architecture and Programming | PE | 3 | 0 | 0 | 3 |
| 8 | P19VL308 | Digital Control Engineering | PE | 3 | 0 | 0 | 3 |

PROGRAM ELECTIVES (PE)





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| | Upon c | completion of this course, students will be able to | | | | | |
| | CO1 | (Apply) Design MOSFET and BJT devices to desired specifications. | | | | | |
| Outcomes | CO2 | (Apply) Model MOSFET and BJT devices to desired specifications. | | | | | |
| | CO3 | (Analyze) Analyze the CMOS Parameters and performance. | | | | | |
| | CO4 | (Apply) Apply the mathematical techniques for device simulations | | | | | |
| | CO5 (Analyze) Analyze concepts about Bipolar Devices. | | | | | | |
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SEMESTER I – ELECTIVE I

MODULE I MOS CAPACITORS

Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in an MOS Structure, Poly-silicon-Gate Work Function and Depletion Effects, MOS under Non-equilibrium and Gated Diodes, Charge in Silicon Dioxide and at the Silicon–Oxide Interface, Effect of Interface Traps and Oxide Charge on Device Characteristics, High-Field Effects, Impact Ionization and Avalanche Breakdown, Band-to-Band Tunneling, Tunneling into and through Silicon Dioxide, Injection of Hot Carriers from Silicon into Silicon Dioxide, High-Field Effects in Gated Diodes, Dielectric Breakdown

MODULE II MOSFET DEVICES

Long-Channel MOSFETs, Drain-Current Model, MOSFET I-V Characteristics, Sub-threshold Characteristics, Substrate Bias and Temperature Dependence of Threshold Voltage, MOSFET Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, Short-Channel MOSFETs, Short-Channel Effect, Velocity Saturation and High-Field Transport Channel Length Degradation and Breakdown at High Fields

MODULE III CMOS DEVICE DESIGN

MOSFET Scaling, Constant-Field Scaling, Generalized Scaling, Non-scaling Effects, Threshold Voltage, Threshold-Voltage Requirement, Channel Profile Design, Non-uniform Doping, Quantum Effect on Threshold Voltage, Discrete Dopant Effects on Threshold Voltage, MOSFET Channel Length, Various Definitions of Channel Length, Extraction of the Effective Channel Length, Physical Meaning of Effective Channel Length, Extraction of Channel Length by C–V Measurements

MODULE IV CMOS PERFORMANCE FACTORS

Basic CMOS Circuit Elements, CMOS Inverters, CMOS NAND and NOR Gates, Inverter and NAND Layouts, Parasitic Elements, Source–Drain Resistance, Parasitic Capacitances, Gate Resistance, Interconnect R and C, Sensitivity of CMOS Delay to Device Parameters, Propagation Delay and Delay Equation, Delay Sensitivity to Channel Width, Length, and Gate Oxide Thickness, Sensitivity of Delay to Power-Supply Voltage and Threshold Voltage, Sensitivity of Delay to Parasitic Resistance and Capacitance, Delay of Two-Way NAND and Body Effect, Performance Factors of Advanced CMOS Devices, MOSFETs in RF Circuits, Effect of Transport Parameters on CMOS Performance, Low-Temperature CMOS

MODULE V BIPOLAR DEVICES

n-p-n Transistors, Basic Operation of a Bipolar Transistor, Modifying the Simple Diode Theory for Describing Bipolar Transistors, Ideal Current-Voltage Characteristics, Collector Current, Base Current, Current Gains, Ideal IC-VCE Characteristics, Characteristics of a Typical n-p-n Transistor, Effect of Emitter and Base Series Resistances, Effect of Base-Collector Voltage on Collector Current, Collector Current Falloff at High Currents, Non-ideal Base Current at Low Currents, Bipolar Device Models for Circuit and Time-Dependent Analyses Basic dc Model, Basic ac Model, Small-Signal Equivalent-Circuit Model, Emitter Diffusion Capacitance, Charge-Control Analysis, Breakdown Voltages, Common-Base Current Gain in the Presence of Base-Collector Junction Avalanche, Saturation Currents in a Transistor, Relation Between BVCEO and BVCBO.

| Total: | 45 HOURS |
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| REFE | REFERENCES | | | | | | |
|------|---|--|--|--|--|--|--|
| 1. | Behzad Razavi, "Fundamentals of Microelectronics" Wiley Student Edition, 2nd Edition. | | | | | | |
| 2. | J P Collinge, C A Collinge, "Physics of Semiconductor devices" Springer 2002 Edition. | | | | | | |
| 3. | Yuan Taur and Tak H. Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, Second Edition. | | | | | | |



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| | Upon o | completion of this course, students will be able to | | | | | | |
| | CO1 | CO1 (Understand) Understand the principles of operation of an RF receiver front end | | | | | | |
| Outcomes | CO2 | CO2 (Apply) Design the constraints for LNAs, Mixers and Frequency synthesizers | | | | | | |
| | CO3 | CO3 (Apply) Apply the constraints for LNAs, Mixers and Frequency synthesizers | | | | | | |
| | CO4 | CO4 (Analyze) Analyze the oscillator and sources of noise. | | | | | | |
| | CO5 (Analyze) Analyze the PLL and frequency Synthesizers. | | | | | | | |
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| MODULE I | IMPE | DANCE MATCHING IN AMPLIFIERS | | | | 9 | | |

Definition of "Q", series parallel transformations of lossy circuits, impedance matching using "L", "PI" and T networks, Integrated inductors, resistors, Capacitors, tunable inductors, transformers

MODULE II AMPLIFIER DESIGN

Noise characteristics of MOS devices, Design of CG LNA and inductor degenerated LNAs. Principles of RF Power Amplifiers design.

MODULE III ACTIVE AND PASSIVE MIXERS

Qualitative Description of the Gilbert Mixer - Conversion Gain, and distortion and noise , analysis of Gilbert Mixer - Switching Mixer - Distortion in Unbalanced Switching Mixer - Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer -Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.

MODULE IV OSCILLATORS

LC Oscillators, Voltage Controlled Oscillators, Ring oscillators, Delay Cells, tuning range in ring oscillators, Tuning in LC oscillators, Tuning sensitivity, Phase Noise in oscillators, sources of phase noise

MODULE V PLL AND FREQUENCY SYNTHESIZERS

Phase Detector/Charge Pump, Analog Phase Detectors, Digital Phase Detectors, Frequency Dividers, Loop Filter Design, Phase Locked Loops, Phase noise in PLL, Loop Bandwidth, Basic Integer-N frequency synthesizer, Basic Fractional-N frequency synthesizer.

Total:

45 HOURS

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- 1. B.Razavi ,"RF Microelectronics" , Prentice-Hall ,1998
- 2. Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002
- 3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits" McGraw-Hill, 1999
- 4. Jia-sheng Hong, "Microstrip filters for RF/Microwave applications", Wiley, 2001
- 5. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits", Cambridge University Press ,2003

| P19VI 303 | DESIG | GN OF ANALOG FILTERS AND SIGNAL CONDITIONING | L | Т | Ρ | С | | | | |
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| | Upon o | pon completion of this course, students will be able to | | | | | | | | |
| | C01 | Apply the operational and design principles for all the in analog filter configurations. | nportar | nt activ | e | K4 | | | | |
| Outcomes | CO2 | CO2 Knowledge of signal conditioning techniques and the necessary guide lines in a Mixed signal IC environment. | | | | | | | | |
| | CO3 | Realize filters based on switched capacitor technique. | | | | К3 | | | | |
| | CO4 | Apply various signal conditioning techniques for interference | ! | | | К3 | | | | |
| | CO5 | Analyze various signal conditioning Circuits. | | | | K4 | | | | |
| | | | | | | | | | | |
| MODULE I | FILTE | FILTER TOPOLOGIES | | | | | | | | |

The Bilinear Transfer Function - Active RC Implementation, Transconductor-C Implementation, Switched Capacitor Implementation, Biquadratic Transfer Function, Active RC implementation, Switched capacitor implementation, High Q, Q peaking and instability, Transconductor-C Implementation, the Digital Biquad.

MODULE II INTEGRATOR REALIZATION

Low pass Filters, Active RC Integrators – Effect of finite Op-Amp Gain Bandwidth Product, Active RC SNR, gm-C Integrators, Discrete Time Integrators.

MODULE III SWITCHED CAPACITOR FILTER REALIZATION

Switched capacitor Technique, Biquadratic SC Filters, SC N-path filters, Finite gain and bandwidth effects, Layout consideration, Noise in SC Filters.

MODULE IV SIGNAL CONDITIONING TECHNIQUES

Interference types and reduction, Signal circuit grounding, Shield grounding, Signal conditioners for capacitive sensors, Noise and Drift in Resistors, Layout Techniques.

MODULE V SIGNAL CONDITIONING CIRCUITS

Isolation Amplifiers, Chopper and Low Drift Amplifiers, Electrometer and Trans-impedance Amplifiers, Charge Amplifiers, Noise in Amplifiers.

Total: 45 HOURS

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- Ramson Pallas-Areny, John G. Webster "Sensors and Signal Conditioning", Wiley Inter science1.Publication, John Wiley & Sons INC, 2001.
- 2. R.Jacob Baker, "CMOS Mixed-Signal Circuit Design", John Wiley & Sons, 2008.
- 3. Schauman, Xiao and Van Valkenburg, "Design of Analog Filters", Oxford University Press, 2009.

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| | Opon c | completion of this course, students will be able to | | |
| | CO1 | (Understand) Understand the VLSI design methodologies and the behind the combinatorial optimization | concept | K2 |
| Outcomes | CO2 | (Understand) Understanding the various types of graph model, layed data structure algorithms | outs and | K2 |
| | CO3 | (Apply) Develop problem solving skills for partitioning and algorithms | routing | К3 |
| | CO4 | (Understand) Understand and simulate the modeling levels | | K2 |
| | CO5 | (Apply) Develop problem solving skills in synthesis process | | K3 |
| | | | | |
| MODULE I | INTRO | DDUCTION TO VLSI DESIGN FLOW | <u> </u> | 9 |
| Introduction to | VLSI Des | ign methodologies, Basics of VLSI design automation tools, Algorithmic | : Graph T | heory |
| and Computati | onal Co | mplexity, Tractable and Intractable problems, General purpose | method | s fo |
| combinatorial of | oumizatio | | | |
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| | | orign rules Broblem formulation Algorithms for constraint gran | | 9 |
| Placement and r | artitionir | a Circuit representation Placement algorithms Partitioning | i compa | CUUI |
| | | ig, circuit representation, nacement algorithms, rurtitioning | | |
| MODULE III | FLOOF | R PLANNING AND ROUTING | | 9 |
| Floor planning o | oncepts, | Shape functions and floorplan sizing, Types of local routing problems | , Area ro | uting |
| Channel routing | , Global r | outing, Algorithms for global routing. | | 5 |
| | | | | |
| MODULE IV | SIMU | LATION AND LOGIC SYNTHESIS | | 9 |
| Simulation, Gat | e-level m | nodeling and simulation, Switch-level modeling and simulation, Comb | inational | Logi |
| Synthesis, Binar | y Decisio | on Diagrams, Two Level Logic Synthesis. | | |
| | | | | |
| MODULE V | HIGH | LEVEL SYNTHESIS | | 9 |
| Hardware mode | ls for hi | gh level synthesis, internal representation, allocation, assignment a | nd sched | uling |
| scheduling algor | ithms, As | ssignment problem, High level transformations. | | |
| | | | | |
| | | Total: 45 H | OURS | |
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| REFERENCES | | | | |
| 1. N.A. Sher | wani, "Ale | gorithms for VLSI Physical Design Automation", Kluwer Academic Publis | shers, 20 | 02. |
| 2. S.H. Gere | z, "Algori | ithms for VLSI Design Automation", John Wiley & Sons, 2002. | | |
| 3. Sadiq M. | Sait, Hab | ib Youssef, "VLSI Physical Design automation: Theory and Practice", V | Vorld Scie | entific |
| 4 Steven M. | Rubin, "C | Computer Aids for VI SI Desian". Addison Wesley Publishina 1987. | | |

SEMESTER I – ELECTIVE II

| | FMRF | DED SYSTEM DESIGN | L | Т | P | С |
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| | Upon c | ompletion of this course, students will be able to | | | | |
| | CO1 | (Understand) Understand the architecture and design of embedded systems | n involv | ed in de | esign | K2 |
| Outcomes | CO2 | (Apply) Program ARM processor | | | | K3 |
| | CO3 | (Understand) Understand the embedded system netw | ork arc | hitectur | e | K2 |
| | CO4 | (Analyze) Analyze the problems in real time embedded systems and its solutions | implem | entatior | ו of | K4 |
| | CO5 | (Understand) Understand the concepts of system des | ign tech | nologie | S | K2 |
| | | | | | | |
| MODULE I | EMBE | DDED SYSTEM OVERVIEW | | | | 9 |
| Embedded Syste | em Overv | view, Design Challenges – Optimizing Design Metrics, D | esign M | lethodol | ogy, R | T-Leve |
| complinational a | na Seque | intial Components, Optimizing Custom Single-Purpose Pr | ocessor | s. | | |
| | GENE | AL AND STNGLE PURPOSE PROCESSOR | | | | 9 |
| Basic Architectu | Ire Pine | lining Superscalar and VIIW architectures Progra | nmer's | view | Devel | onmen |
| Environment, Ar | polication | -Specific Instruction-Set Processors (ASIPs) Microcontr | ollers. | Timers. | Count | ers an |
| watchdog Timer, | UART, L | CD Controllers and Analog-to-Digital Converters, Memor | v Conce | epts. | count | |
| | · · · · · · , - | | , | P | | |
| MODULE III | BUS S | TRUCTURES | | | | 9 |
| Basic Protocol C | oncepts, | Microprocessor Interfacing – I/O Addressing, Port and | Bus-Ba | ased I/(| D, Arbi | itration |
| Serial Protocols, | , I2C, C | AN and USB, Parallel Protocols – PCI and ARM Bus, | Wirele | ss Prot | ocols | – IrDA |
| Bluetooth, IEEE | 802.11. | | | | | |
| | | | | | | |
| MODULE IV | STATE | MACHINE AND CONCURRENT PROCESS MODELS | | | | 9 |
| Basic State Macl | nine Mod | el, Finite-State Machine with Datapath Model, Capturing | State I | Machine | in Sec | quentia |
| Programming La | anguage, | Program-State Machine Model, Concurrent Process M | odel, Co | ommuni | cation | among |
| Vorification : Ha | rdwaro/S | off among processes, Datanow Model, Real-time Syste | enis, Au | an Proc | ni: Syi | dole |
| | iuware/5 | onware co-simulation, Reuse. Intellectual Property core | s, Desi | girrioc | 233 110 | ueis. |
| | FMRF | DED SOFTWARE DEVELOPMENT TOOLS AND BTOS | | | | 9 |
| Compilation Pro | ress – I | ibraries - Porting kernels - C extensions for embedde | d syste | ems – e | emulat | ion and |
| debuaaina techn | iaues – F | RTOS – System design using RTOS. | | | Sinaiae | |
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| | | | Т | otal: 4! | 5 HOU | RS |
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| REFERENCES | | | | | | |
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| 1. Bruce Pow systems", | vel Doug 3rd Editi | las, "Real time UML, second edition: Developing effi on 1999, Pearson Education. | cient ol | ojects f | or em | bedded |
| 2. Daniel W. Education, | Lewis, 2002. | "Fundamentals of embedded software where C and | assem | nbly me | eet", F | 'earsor |
| 3. Frank Vah | id and To | ny Gwargie, "Embedded System Design", John Wiley & s | sons, 20 | 02. | | |

4. Steve Heath, "Embedded System Design", Elsevier, Second Edition, 2004.

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| | ADVAI | NCED MICROPROCESSORS AND ARCHITECTURES | 3 | 0 | 0 | 3 |
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| | Upon c | ompletion of this course, students will be able to | | | | |
| | CO1 | (Understand) Understand the fundamentals and arch family of 80x86 microprocessors | itecture | of Intel | | K2 |
| Outcomes | CO2 | (Understand) Understand the CISC and RISC archite | cture | | | K2 |
| • | CO3 | (Understand) Understand ARM architecture and proc | essors | | | K2 |
| | CO4 | (Apply) Program ARM microcontrollers | | | | К3 |
| | CO5 | (Understand) Know the CPU architecture of PIC and microcontroller | Motorola | 1 | | K2 |
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| MODULE I | 80386 | AND PENTIUM PROCESSOR | | | | 9 |
| MODULE II Introduction | to RISC a | ND RISC ARCHITECTURE rchitectures: RISC Versus CISC – RISC Case studies: | MIPS R | 4000 - | SPARC | 9 – Inte |
| | 5,0000. | | | | | |
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| Pipelines – E Introduction | xception \ to ARM Me | del – Registers – Processor Modes – State of the proce /ector Table – ARM Processor Families – Typical 3 stag emory Management Unit. | e pipelir | Conditio ied ARM | n Flags organ | ization- |
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| Upon completion of this course, students will be able to Cutcomes CO1 (Understand) Describe continuous time and discrete time controllers analytically. K2 Outcomes CO2 (Understand) Define and state basic analog to digital and digital to analog conversion principles K2 CO3 (Analyze) Analyze sampled data control system in time and frequency domains. K4 CO4 (Apply) Design simple PI, PD, PID continuous and digital controllers. K3 MODULE I CONTROLLERS IN FEEDBACK SYSTEMS 9 Review of frequency and time response analysis and specifications of first order and second order feedback control systems, need for controllers, continuous time compensations, continuous time PI, PD, PID controllers, digital PID controllers. 9 MODULE II BASIC DIGITAL SIGNAL PROCESSING IN CONTROL SYSTEMS 9 Sampling theorem, quantization, aliasing and quantization error, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction. 9 MODULE II MODULE OF SAMPLED DATA CONTROL SYSTEM 9 Difference equation description, first companion, second companion, Jordan canonical models, discrete state variable models (elementary principles only). 9 MODULE IV DESIGN OF DIGITAL CONTROL ALGORITHMS | 3 0 0 | | | | | | |
| Upon completion of this course, students will be able to Cutcomes C01 (Understand) Describe continuous time and discrete K2 Cutcomes C02 (Understand) Define and state basic analog to digital and digital to analycically. K2 C03 (Analyze) Analyze sampled data control system in time and frequency domains. K3 C04 (Apply) Develop schemes for practical implementation of temperature and motor control systems. K3 MODULE I CONTROLLERS IN FEEDBACK SYSTEMS 9 Review of frequency and time response analysis and specifications of first order and second order feedback control systems, need for controllers, continuous time compensations, continuous time PI, PD, PID controllers, digital PID controllers. 9 Sampling theorem, quantization, aliasing and quantization error, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction. 9 MODULE III MODELING OF SAMPLED DATA CONTROL SYSTEM 9 Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury's stability test, state space description, first companion, second companion, Jordan cannical models, discrete state variable models (elementary principles only). 9 | | | | | | | |
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| MODULE III MODELING OF SAMPLED DATA CONTROL SYSTEM 9 Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury's stability test, state space description, first companion, second companion, Jordan canonical models, discrete state variable models (elementary principles only). P MODULE IV DESIGN OF DIGITAL CONTROL ALGORITHMS 9 Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane. 9 MODULE V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS 9 Algorithm development of PID control algorithms, standard programmes for microcontroller implementation, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, micro control systems, micro control systems, micro control systems, micro control system. 9 1 John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill, 1995. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996. Penram International, 2nd Edition, 1996. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997. | | | | | | | |
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| models (elementary principles only). DESIGN OF DIGITAL CONTROL ALGORITHMS 9 Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane. 9 MODULE V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS 9 Algorithm development of PID control algorithms, standard programmes for microcontroller implementation, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems, DSP implementation of motor control system. 9 REFERENCES I. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill, 1995. 2. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996. 3. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997. | frequency respo state space desc | nse of di cription, f | scription, 2-transform method of description, pulse screte time control systems, stability of digital control s first companion, second companion, Jordan canonical m | transfer systems lodels, d | s, Jury's discrete | stabilit state v | ie and sy test, ariable |
| MODULE IV DESIGN OF DIGITAL CONTROL ALGORITHMS 9 Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane. 9 MODULE V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS 9 Algorithm development of PID control algorithms, standard programmes for microcontroller implementation, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems, DSP implementation of motor control system. 9 REFERENCES I John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill, 1995. 8 2. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996. 9 3. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997. | models (element | tary princ | ciples only). | | | | |
| Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane. MODULE V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS 9 Algorithm development of PID control algorithms, standard programmes for microcontroller implementation, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems, DSP implementation of motor control system. Total: 45 HOURS REFERENCES 1. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill, 1995. 2. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996. 3. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997. | | DESIC | | | | | 0 |
| Review of principle of compensator design, 2 plane specifications, digital compensator design during inequerely response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane. MODULE V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS 9 Algorithm development of PID control algorithms, standard programmes for microcontroller implementation, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems, DSP implementation of motor control system. Image: References Image: Total: 45 HOURS Image: Normalized System Analysis and Design", Mc Graw Hill, 1995. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996. Image: McGopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997. | Review of princip | | nnensator design Z-plane specifications digital comper | sator d | ocian us | sing free | |
| MODULE V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS 9 Algorithm development of PID control algorithms, standard programmes for microcontroller implementation, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems, DSP implementation of motor control system. Total: 45 HOURS REFERENCES 1. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill, 1995. 2. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996. 3. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997. | response plots, function, design | discrete in the Z- | integrator, discrete differentiator, development of di- plane. | gital PI | D contr | oller, t | ransfer |
| Algorithm development of PID control algorithms, standard programmes for microcontroller implementation, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems, DSP implementation of motor control system. Total: 45 HOURS REFERENCES 1. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill, 1995. 2. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996. 3. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997. | MODULE V | PRACT | ICAL ASPECTS OF DIGITAL CONTROL ALGORITHM | s | | | 9 |
| finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems, DSP implementation of motor control system. Total: 45 HOURS REFERENCES 1. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill, 1995. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996. 3. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997. | Algorithm develo | opment o | of PID control algorithms, standard programmes for min | _ crocontr | oller im | plemen | - itation. |
| systems, microcontroller based motor speed control systems, DSP implementation of motor control system. Total: 45 HOURS REFERENCES 1. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill,1995. 2. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996. 3. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997. | finite word leng | th effect | s, choice of data acquisition systems, microcontroller | based | tempe | rature | control |
| Total: 45 HOURS REFENCES 1. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill, 1995. 2. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996. 3. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997. | systems, microc | ontroller | based motor speed control systems, DSP implementatio | n of mo | tor cont | rol syst | em. |
| Total: 45 HOURS REFERENCES 1. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill,1995. 2. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996. 3. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997. | | | | | | | |
| REFERENCES 1. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill,1995. 2. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996. 3. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997. | | | Total: | | 45 H | OURS | |
| REFERENCES 1. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill,1995. 2. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996. 3. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997. | | | | | | | |
| John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill,1995. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997. | REFERENCES | | | | | | |
| Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997. | 1. John J. D' | Azzo, "Co | nstantive Houpios, Linear Control System Analysis and I | Design", | Mc Gra | w Hill,1 | 995. |
| 3. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997. | 2. Kenneth J Penram In | . Ayala, " Iternatior | The 8051 Microcontroller- Architecture, Programming ar al, 2nd Edition, 1996. | nd Appli | cations" | 1 | |
| | 3. M.Gopal, ' | 'Digital C | ontrol and Static Variable Methods", Tata McGraw Hill, N | ew Delł | ni, 1997 | | |

| SI.No. | Course Code | Course Title | Category | Contact Periods | L | т | Ρ | С |
|---------|----------------|---------------------------|----------|--------------------|----|---|---|----|
| THEORY | | | | | | | | |
| 1 | P19VL104 | Analog IC Design | PC | 4 | 4 | 0 | 0 | 4 |
| 2 | P19VL105 | Low Power VLSI Design | PC | 3 | 3 | 0 | 0 | 3 |
| 3 | P19VL106 | Testing of VLSI Circuits | PC | 3 | 3 | 0 | 0 | 3 |
| 4 | P19VL3XX | Program Elective III | PE | 3 | 3 | 0 | 0 | 3 |
| 5 | P19VL3XX | Program Elective IV | PE | 3 | 3 | 0 | 0 | 3 |
| PRACTIC | ALS | | | | | | | |
| 6 | P19VL112 | VLSI Design Laboratory II | PC | 4 | 0 | 0 | 4 | 2 |
| 7 | P19VL201 | Mini Project | PW | 4 | 0 | 0 | 4 | 2 |
| 8 | P19AC5XX | Audit Course II | AC | 2 | 2 | 0 | 0 | NC |
| | | TOTAL | | 26 | 18 | 0 | 8 | 20 |

Semester II

Leadership & Excellence



| 10// 104 | | | STON | | | | | | | L | Т | Р | С |
|--|---|---|--|-----------------------------|---|---|--|--|---------------------------------------|-----------------------------|--------------------|---------------------|--------------------|
| 1971104 | ANALC | GIC DES | | | | | | | | 3 | 0 | 0 | 3 |
| | Upon c | ompletion | of this | | irse, sti | idents w | ill be a | ble to | | | | | |
| | | (Analyz | οι απο | | s single | stane a | nnlifiar | s with | MOSI | oads | | | K4 |
| | 001 | (Analyzo | ε) Δn | alvz | e the | concent | s of f | requer | nos re | snonse | and | noise | |
| Outcomes | CO2 | character | ristics | of di | fferenti | al ampli | iers. | requei | icy ic | sponse | unu | noise | K4 |
| | CO3 | (Apply) | Desigr | n an | d model | differer | nt activ | e devic | es wit | h OPAM | Ps. | | K3 |
| | CO4 | (Unders compens | tand) ations | In tech | iterpret iniques. | the | multi-p | ole sy | ystems | s, freq | uency | | K2 |
| | CO5 | (Apply) | Desigr | n ana | alog ciro | uits usi | ng CMC | S tech | nology | /. | | | K3 |
| MODULE-I | MOSFE | T METRI | CS | | | | | | | | | | 9 |
| transistor theory conduction, Reli Miller"s approxim | , Short c ability, D nation | hannel efi igital met | fects, trics, / | Narr Anal | ow wid og met | th effec rics, Sr | :, Drair nall sig | n induc gnal pa | ed ba arame | rrier lov ters, Ui | vering, nity Ga | Sub-th ain Frea | resholo quency |
| | SING | E STAGE | | rwo | STAG | | FTFR | | | | | | 9 |
| Single Stage Am | plifiers - | Commor | n sourc | ce a | mplifier | with re | sistive | load, | diode | load, c | onstant | currer | nt load |
| Source degenera | ation Sou | rce follow | ver, In | put | and ou | tput im | pedanc | e, Cor | nmon | gate a | mplifier | - Diff | erentia |
| Amplifiers – diffe | rential ar | nd commo | n mod | le re | sponse, | Input s | wing, g | gain, di | ode lo | ad and | constai | nt curre | ent load |
| - Basic Two Stag | e Amplifie | er, Cut-off | freque | ency | , poles | and zero | os | | | | | | |
| | FREQU | | CDON | CF (| | | | | 0 CT 4 | | | DC | • |
| Frequency Respo | nse of S | ingle Stac | ie Amr | Jifie | rs - No | ise in S | inale s | tage A | mplifie | ers – St | ability a | and Fre | equency |
| Compensation in Amplifiers – Sta loading in feedba | Single s bility, gai ck netwo | age Ampl n and ph rks | lifiers, ase m | Frec argi | quency ns, Fred | Respons Juency | e of Ty Compe | vo Stag nsation | ge Am in tw | plifiers, o stage | – Nois Ampli | e in tw fiers, E | o stage ffect o |
| | | | | | | | | | | | | | _ |
| MODULE-IV | | | | | REFER | | | IS Voltag | o rofo | ron co (| Constar | t Cm I | 9 hincing |
| supply and tem mismatch in anal | perature og desigr | independ | lent re | efere | ence, c | urvature | comp | ensatio | on, tri | mming, | Effect | of tra | ansisto |
| | | DC | | | | | | | | | | | 0 |
| Gilbert cell and | applicat | ions. Bas | ic two |) sta | age OP | AMP. tv | o-nole | syste | m res | sponse | comm | on mo | de and |
| differential gain, | Frequer | cy respon | nse of | OP | AMP, C | MFB cir | cuits, | slew ra | ate, p | ower si | upply r | ejectior | n ratio |
| random offset, s | /stematic | offset, No | oise, O | utpu | ut stage | , OTA ar | nd OPA | MP circ | uits - | Low vol | tage OF | PAMP | |
| | | | | | | | | | | | | | |
| | | | | | | | | Т | otal: | | 45 H | OURS | |
| | | | | | | | | | | | | | |
| DEEEDENCES | | | | | | | | | | | | | |
| REFERENCES. | | | | | | | | | | | | | |
| 1. Behzad Ra | zavi, "De | sign of An | alog C | MOS | 5 Integra | ated Cire | cuits", l | McGrav | v Hill, | 2000 | | | |
| 1.Behzad Ra2.Philip E.All | zavi, "De en, "CMO | sign of An S Analog | alog C Circuit | MOS Des | 5 Integra sign", O | ated Circ (ford Ur | cuits", l iversity | McGrav v Press | v Hill, , 2013 | 2000 | | | |
| 1. Behzad Ra 2. Philip E.All 3. Paul R.Gra | zavi, "De en, "CMO ıy, "Analy | sign of An S Analog 'sis and D | alog C Circuit Design | MOS Des of A | S Integra sign", Os Analog I | ated Ciro (ford Ur Integrat | cuits", l iversity ed Circ | McGrav Press uits", V | v Hill, , 2013 Wiley | 2000 Student | edition | n, 5th (| edition |
| 1.Behzad Ra2.Philip E.All3.Paul R.Gra2009.4.4.R.Jacob Ba | zavi, "De en, "CMO ıy, "Analy ıker, "CM | sign of An S Analog 'sis and E DS: Circui | alog C Circuit Design t Desig | MOS Des of A | S Integra sign", Os Analog S avout | ated Circ kford Ur Integrat and Sin | cuits", l iversity ed Circ | McGrav v Press uits", N uits", Wile | v Hill, , 2013 Wiley ev Stud | 2000 Student dent Edi | edition | n, 5th (009 | edition |
| 1.Behzad Ra2.Philip E.All3.Paul R.Gra2009.4.4.R.Jacob Ba5.Willey M.C | zavi, "De en, "CMO iy, "Analy iker, "CM . Sansen, | sign of An S Analog 'sis and E 'SS: Circui '`Analog o | alog C Circuit Design t Desig design | MOS Des of A gn, L | G Integra sign", O: Analog I Layout , entials", | ated Circ kford Ur Integrat and Sin Springe | cuits", l iversity ed Circ nulation er, 2000 | McGrav Press, uits", N n", Wile 5. | v Hill, , 2013 Wiley ey Stud | 2000 Student dent Edi | edition, 20 | n, 5th (009 | edition |

| P19VL105 | LOW | POWER VLSI DESIGN | - | P | L. |
|---|--|--|--|--|---------------------------------------|
| | | 3 | 0 | 0 | 3 |
| | Upon | completion of this course, students will be able to | | | |
| | CO1 | (Apply) Identify the sources of power dissipation in digital | IC syst | ems. | КЗ |
| | 001 | Understand the impact of power on system performance and r | eliabilit | y | |
| | CO2 | (Analyze) Examine various power optimization algorithms in | n low p | ower | К4 |
| Outcomes | | VLSI design system | | | |
| | CO3 | (Apply) Design of low power CMOS circuits | | | K3 |
| | CO4 | (Apply) Apply probabilistic analysis to characterize dyna | amic p | ower | К3 |
| | | estimation | | | |
| | CO5 | (Apply) Design low power VLSI circuits and apply the te | echnique | es in | K3 |
| | | different applications. | | | |
| | DOM/ | D DISSIDATION IN CMOS | | | 0 |
| hysics of p | wer dissin | ation in CMOS FET devices – Hierarchy of limits of power - | - Sourc | res of | y nowe |
| consumption | – Static F | ower Dissipation, Active Power Dissipation - Designing for | Low Po | ower, (| Circui |
| rechniques F | or Leakage | Power Reduction - Basic principle of low power design. | | , | |
| | | | | | |
| MODULE-II | POWE | R OPTIMIZATION | | | 9 |
| _ogic level p Architectures | ower optim BiCMOS ac | ders - Low Voltage Low Power Design Techniques, Current Mod | Lelis, L do Adde | MUS A | ader |
| Alchitectules | DICINOS ac | ders - Low voltage Low rower Design rechniques, Current not | le Auue | 15 - I y F | |
| Multiplier Arc | nitectures, I | Braun, Booth and Wallace Tree Multipliers and their performance | e compa | rison | |
| Multiplier Arc | nitectures, I | Braun, Booth and Wallace Tree Multipliers and their performance | e compa | rison | |
| Multiplier Arc | nitectures, l | Braun, Booth and Wallace Tree Multipliers and their performance | e compa | rison | 9 |
| Multiplier Arc MODULE III Computer ari | DESIC DESIC | Braun, Booth and Wallace Tree Multipliers and their performance GN OF LOW POWER CMOS CIRCUITS hniques for low power system – low voltage low power static | Randon | n acces | 9 s an |
| Multiplier Arc MODULE III Computer ari dynamic Ran | DESIC DESIC thmetic tec dom acces | Braun, Booth and Wallace Tree Multipliers and their performance SN OF LOW POWER CMOS CIRCUITS hniques for low power system – low voltage low power static s memories – low power clock, Inter connect and layout | Randon design | n acces - Adv | 9 s and ance |
| Multiplier Arc MODULE III Computer ari dynamic Ran techniques – | DESIC DESIC thmetic tec dom acces Special tech | Braun, Booth and Wallace Tree Multipliers and their performance SN OF LOW POWER CMOS CIRCUITS hniques for low power system – low voltage low power static s memories – low power clock, Inter connect and layout nniques. | Randon design | n acces - Adv | 9 s an ance |
| Multiplier Arc MODULE III Computer ari dynamic Ran techniques – MODULE IV | DESIC DESIC thmetic tec dom acces Special tech | Braun, Booth and Wallace Tree Multipliers and their performance GN OF LOW POWER CMOS CIRCUITS hniques for low power system – low voltage low power static s memories – low power clock, Inter connect and layout hniques. R ESTIMATION | Randon design | n acces - Adv | 9 s an ance 9 |
| Multiplier Arc MODULE III Computer ari dynamic Ran cechniques – MODULE IV Power Estima | DESIC DESIC thmetic tec dom acces Special tech POWE ttion techni | Braun, Booth and Wallace Tree Multipliers and their performance SN OF LOW POWER CMOS CIRCUITS hniques for low power system – low voltage low power static s memories – low power clock, Inter connect and layout iniques. R ESTIMATION ques – logic power estimation – Simulation power analysis | Randon design -Probal | n acces – Adv pilistic | 9 ss an ance 9 powe |
| Multiplier Arc MODULE III Computer ari dynamic Ran cechniques – MODULE IV Power Estima analysis. | DESIC DESIC thmetic tec dom acces Special tech POWE tion techni | Braun, Booth and Wallace Tree Multipliers and their performance SN OF LOW POWER CMOS CIRCUITS hniques for low power system – low voltage low power static s memories – low power clock, Inter connect and layout iniques. R ESTIMATION ques – logic power estimation – Simulation power analysis | Randon design -Probal | n acces – Adv pilistic | 9 ance 9 powe |
| Multiplier Arc MODULE III Computer ari dynamic Ran cechniques – MODULE IV Power Estima analysis. | DESIC DESIC thmetic tec dom acces Special tech POWE ation techni | Braun, Booth and Wallace Tree Multipliers and their performance GN OF LOW POWER CMOS CIRCUITS hniques for low power system – low voltage low power static is memories – low power clock, Inter connect and layout iniques. R ESTIMATION ques – logic power estimation – Simulation power analysis | Randon design -Probal | n acces – Adv pilistic | 9 ss and anced 9 powe |
| Multiplier Arc MODULE III Computer ari dynamic Ran echniques – MODULE IV Power Estima analysis. | DESIC DESIC thmetic tec dom acces Special tech POWE ation techni SYNT | Braun, Booth and Wallace Tree Multipliers and their performance SN OF LOW POWER CMOS CIRCUITS hniques for low power system – low voltage low power static s memories – low power clock, Inter connect and layout iniques. IR ESTIMATION ques – logic power estimation – Simulation power analysis HESIS AND SOFTWARE DESIGN FOR LOW POWER – Bobavioral loyal transform – software dosign for low power | Randon design -Probal | n acces – Adv pilistic | 9 ance 9 powe 9 |
| Multiplier Arc MODULE III Computer ari dynamic Ran echniques – MODULE IV Power Estima analysis. MODULE V Synthesis for | bitectures, I DESIC thmetic tec dom acces Special tech POWE ation technic SYNT low power | Braun, Booth and Wallace Tree Multipliers and their performance SN OF LOW POWER CMOS CIRCUITS hniques for low power system – low voltage low power static s memories – low power clock, Inter connect and layout nniques. R ESTIMATION ques – logic power estimation – Simulation power analysis HESIS AND SOFTWARE DESIGN FOR LOW POWER - Behavioral level transform – software design for low power. | Randon design -Probal | n acces – Adv pilistic | 9 ss and ance 9 powe 9 |
| Multiplier Arc MODULE III Computer ari dynamic Ran echniques – MODULE IV Power Estima analysis. MODULE V Synthesis for | DESIC DESIC thmetic tec dom acces Special tech tion techni SYNT low power | Braun, Booth and Wallace Tree Multipliers and their performance SN OF LOW POWER CMOS CIRCUITS hniques for low power system – low voltage low power static s memories – low power clock, Inter connect and layout iniques. R ESTIMATION ques – logic power estimation – Simulation power analysis HESIS AND SOFTWARE DESIGN FOR LOW POWER - Behavioral level transform – software design for low power. | Randon design -Probal | n acces – Adv pilistic | 9 ance 9 powe 9 |
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| D10VI 106 | TECTI | | L | Т | Р | С |
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| P19VL100 | 12311 | | 3 | 0 | 0 | 3 |
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| | Upon o | completion of this course, students will be able to | | | | |
| | CO1 | (Understand) Interpret the importance of testing and circuits | d its typ | es in VL | SI | K2 |
| 0.1 | CO2 | (Analyze) Analyze the testing of sequential and comb | inationa | l circuits | 5 | K4 |
| Outcomes | CO3 | (Apply) Model different faults and carry out fault sin circuits | mulatior | ı in digi | ital | К3 |
| | CO4 | (Apply) Determine fault oriented test vectors for sine in combinational and Sequential circuits. | gle stuc | k-at-fau | ılts | К3 |
| | CO5 | (Apply) Design digital VLSI circuits with DFT and BIST | technic | lues | | K3 |
| | | | | | | |

MODULE I TESTING AND FAULT MODELLING

Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation –Delay models – Gate Level Event – driven simulation.

MODULE II TEST GENERATION

Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.

MODULE III DESIGN FOR TESTABILITY

Design for Testability – Ad-hoc design – generic scan based design – classical scan based design– system level DFT approaches.

MODULE IV SELF – TEST AND TEST ALGORITHMS

Built-In self-test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.

MODULE V FAULT DIAGNOSIS

Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits– Selfchecking design – System Level Diagnosis.

Total: 45 HOURS

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- 1. A.L.Crouch, "Design Test for Digital IC"s and Embedded Core Systems", Prentice Hall International, 2002.
- 2. M.Abramovici, M.A.Breuer and A.D. Friedman, "Digital systems and Testable Design", Jaico Publishing House, 2002.
- 3. M.L.Bushnell and V.D.Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed- Signal VLSI Circuits", Kluwer Academic Publishers, 2002.
- 4. P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.

| D10 | VI 112 | | ocian Laboratory II | L | Т | Р | С | | | | |
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| P19 | VLIIZ | VLSIL | | 0 | 0 | 4 | 2 | | | | |
| | | Upon c | ompletion of this course, students will be ab | etion of this course, students will be able to | | | | | | | |
| Out | comes | CO1 | Carryout a complete VLSI based exper TANNER / Mentor / Synopsis | riments usin | g / CAE | DENCE / | К3 | | | | |
| | | | List of Experiments | | | | | | | | |
| 1. | To synthes | size and | understand the Boolean optimization in synt | hesis. | | | | | | | |
| 2. | Static timi | ng analy | ses procedures and constraints. | | | | | | | | |
| 3. | Critical path considerations. Scan chain insertion, Floor planning, Routing and Placeme procedures. | | | | | | | | | | |
| 4. | Power plar | nning, La | yout generation, LVS and back annotation, | Total power | estimate. | | | | | | |
| 5. | Analog cir amplifier i | cuit sim n Spice. | Ilation. Simulation of logic gates, Current | mirrors, Cur | rent sou | rces, Diff | erential | | | | |
| 6. | Layout ger | nerations | , LVS, Back annotation p & Exceller | 108 | | | | | | | |
| | | | | | Tot | al: 45 H | IOURS | | | | |
| REFERE | ENCES | | | | | | | | | | |
| 1. | Ming-Bo Li | in, Digita | l System Designs and Practices us <mark>ing Verilo</mark> | <mark>g HD</mark> L and FI | PGAs, Wil | ey, 2012. | | | | | |
| 2. | Samir Palr | nitkar, Ve | rilog HDL, Pearson Education, 2 <mark>ndEdition, 2</mark> | . <mark>0</mark> 04. | | | | | | | |
| 3. | J.Bhaskar, | A VHDL | Primer, Prentice Hall, 1998. | | | | | | | | |
| 4. | M.H.Rashid, Spice for Circuits and Electronics using Pspice, PHI 1995. | | | | | | | | | | |
| 5. | M.J.S.Smit | th, Appli | ation Specific Integrated Circuits, Pearson E | Education, 20 | 08. | | | | | | |

| SI.No | Course Code | Course Title | Course Category | L | т | Ρ | С |
|-------|----------------|--|--------------------|---|---|---|---|
| | | SEMESTER II – ELECTIVE III | | | | | |
| 1 | P19VL309 | DSP Integrated Circuits | PE | 3 | 0 | 0 | 3 |
| 2 | P19VL310 | VLSI Signal Processing | PE | 3 | 0 | 0 | 3 |
| 3 | P19VL311 | Soft Computing and Optimization Techniques | PE | 3 | 0 | 0 | 3 |
| 4 | P19VL312 | Reconfigurable Architectures | PE | 3 | 0 | 0 | 3 |
| | | SEMESTER II – ELECTIVE IV | | | | | |
| 1 | P19VL313 | CMOS Digital VLSI Design | PE | 3 | 0 | 0 | 3 |
| 2 | P19VL314 | Networks on Chip | PE | 3 | 0 | 0 | 3 |
| 3 | P19VL315 | Design and Analysis of Computer Algorithms | PE | 3 | 0 | 0 | 3 |
| 4 | P19VL316 | Digital Image Processing | PE | 3 | 0 | 0 | 3 |

PROGRAM ELECTIVES (PE)



SEMESTER II - ELECTIVE III

| D101/1 200 | | TEGRATED CIRCUITS | | Т | Ρ | С | |
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| P19VL309 | D3P I | | | 0 | 0 | 3 | |
| | | | | | | | |
| | Upon o | completion of this course, students will be able to | | | | | |
| | CO1 | CO1 (Understand) Get to know about the Digital Signal Processing concepts and its algorithms | | | | | |
| Outcomes | CO2 | (Understand) Get an idea about finite word length effects in digital filters | | | | | |
| | CO3 | O3 (Understand) Understand the concepts of multirate systems | | | | | |
| | CO4 | (Understand) Familiarize with the DSP processor architecture | | | | | |
| | CO5 | (Apply) Implementation of digital signal processing ar systems | nd Numb | er | | К3 | |
| | | | | | | | |

MODULE I **INTRODUCTION TO DSP INTEGRATED CIRCUITS**

Introduction to Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signalprocessing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT Algorithm, Image coding, Discrete cosine transforms, Standard digital signal processors, Application specific ICs for DSP, DSP systems, DSP system design, Integrated circuit design.

DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS MODULE II

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multi rate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multi rate filters. Finite word length effects - Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

MODULE III DSP ARCHITECTURES

DSP system architectures, Standard DSP architecture-Harvard and Modified Harvard architecture. Ideal DSP architectures, Multiprocessors and multi computers, Systolic and Wave front arrays, Shared memory architectures.

MODULE IV SYNTHESIS OF DSP ARCHITECTURES

Synthesis: Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit - serial PEs. Combinational & sequential networks- Storage elements - clocking of synchronous systems, Asynchronous systems -FSM

MODULE V **ARITHMETIC UNIT AND PROCESSING ELEMENTS**

Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Digit Serial arithmetic, CORDIC Algorithm, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Case Study: DCT and FFT processor

Total: 45 HOURS

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| 1. | B.Venkatramani, M.Bhaskar, "Digital Signal Processors", Tata McGraw-Hill, 2002 |
|----|--|
| 2. | John J. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", Pearson Education, 2002 |
| 3. | Keshab Parhi, "VLSI Digital Signal Processing Systems design & Implementation", John Wiley & Sons, 1999. |
| Λ | Lars Wanhammer "DSP Integrated Circuits" Academic press, New York, 1999 |

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| P1 | 9VL310 | VLSI Signal Processing | | 3 | 0 | 0 | 3 |
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| | | Upon c | completion of this course, students will be able to | | | | |
| | | C01 | (Understand) Represent DSP algorithms, define iteration bound of an algorithm. | and | compute | 9 | K2 |
| Ou | itcomes | CO2 | (Apply) Use Pipelining and parallel processing meth- filters | odologi | es in FII | ٤ | К3 |
| | | CO3 | (Apply) Apply retiming, unfolding techniques. | | | | K3 |
| | | CO4 | (Apply) Design systolic architecture. | | | | K3 |
| | | CO5 | (Apply) Apply strength reduction in filters and transfor | ms. | | | K3 |
| | | | | | | | |
| MOD | ULE I | PIPEL | INING AND PARALLEL PROCESSING OF DIGITAL FI | LTERS | | | 9 |
| boun Pipeli | d, iteration ning and Pa | bound, rallel pro | Longest path matrix algorithm, Pipelining and Parall ocessing for low power. | el proc | essing o | f FIR | filters, |
| MOD | | | | | | | |
| Datim | ULE II | ALGO | d proportion Unfolding on placetithm for unfolding on | | | dina | 9 |
| MOD Fast filters | ULE III convolution s – Look-Ah | ALGOI - Cook | RITHIMIC STRENGTH REDUCTION -II Toom algorithm, modified Cook-Toom algorithm, Pipe Plining in first-order IIR filters, Look-Ahead pipelining wi elining Parallel processing of IIR filters, combined pipel | elined a th powe | and para erof-2 de | llel re ecompo | 9 cursive |
| of IIF | tilters. | | | | | | |
| MOD | ULE IV | BIT-LI | EVEL ARITHMETIC ARCHITECTURES | | | | 9 |
| Bit-le multi CSD FIR fi | vel arithmet pliers, Desig multiplicatio lters ULE V | tic archit In of Lyc In using NUME | RICAL STRENGTH REDUCTION, WAVE AND AS | el carry IR filter Arithme SYNCH I | -ripple an , CSD re tic funda RONOUS | nd carr preser amenta | y-save itation ils and |
| | | PIPEL | INING | | | | |
| Nume synch clock | erical streng nronous pipe ing, wave pi | th reduc elining a pelining | tion – subexpression elimination, multiple constant mult and clocking styles, clock skew in edge-triggered single Asynchronous pipelining bundled data versus dual rail p | iplicatio e phase protocol | on, iterati e clockin | ve ma g, two | tching, -phase |
| | | | Total: | | 45 HC | URS | |
| REFE | RENCES | | | | | | |
| 1. | Keshab K. Interscienc | Parhi, e, 2007 | "VLSI Digital Signal Processing Systems, Design a | nd imp | lementa | tion", | Wiley, |
| 2. | U. Meyer - Edition, 20 | - Baese, 04. | "Digital Signal Processing with Field Programmable Gat | te Array | /s″, Spriı | nger, S | Second |

| P19VL311 | | SOFT COMPUTING AND OPTIMIZATION TECHNIOUES | | | т | | Ρ | С | | |
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| | | Linon c | ompletion of this course, students will be able to | | | | | | | |
| | | oponic | supretion of this course, statents will be able to | | | | | | | |
| | | CO1 | (Apply) Implement machine learning through Neural | netwo | rks. | | | К3 | | |
| Our | tcomes | CO2 (Apply) Develop a Fuzzy expert system. | | | | | | | | |
| ••• | ceenies | CO3 (Apply) Model Neuro Fuzzy system for clustering and classification. | | | | | | | | |
| | | CO4 (Apply) Use the optimization techniques to solve the real world K3 problems | | | | | | | | |
| | | CO5 | (Analyze) Analyze the Genetic algorithm and its opti | mizatio | n | | | K4 | | |
| MODI | | NEUR | | | | | - | 9 | | |
| Machi | ne Learning | g using l | Jeural Network, Learning algorithms, Supervised Lear | ning N | eural N | etwo | ·ks – | Feed | | |
| Forwa | ard Network | ks, Radia | I Basis Function, Unsupervised Learning Neural Netw | orks - | Self C | Organi | zing | map, | | |
| Adapt | ive Resona | nce Arch | tectures, Hopfield network | | | | | | | |
| MODI | | EU77V | | | | | | 0 | | |
| Fuzzy | Sets – Op | erations | on Fuzzy Sets - Fuzzy Relations - Membership Fund | tions-l | Fuzzv R | lules | and I | Fuzzv | | |
| Reaso | oning – Fuzz | y Infere | nce Systems – Fuzzy Expert Systems – Fuzzy Decision | Making |]] | | | , | | |
| | | | | | | | | | | |
| MOD | | NEUR | O-FUZZY MODELING | | | | | 9 | | |
| Adapt | IVE Neuro-I – Data Clui | -uzzy In sterina A | erence Systems - Coactive Neuro-Fuzzy Modeling - | Classif Fuzzy (| | | kegre o Sti | SSION | | |
| nees | Data Ciu. | stering P | | uzzy (| Source | Cus | | uics. | | |
| MOD | ULE IV | CONV | INTIONAL OPTIMIZATION TECHNIQUES | | | | | 9 | | |
| Introc | luction to o | ptimizat | on techniques, Statement of an optimization problem | classi | fication | , Unc | onstr | ained | | |
| optim | ization-grad | dient sea | rch method-Gradient of a function, steepest gradient- | conjug | ate gra | dient | New | /ton's | | |
| function | on method | externa | log, Constrained optimization -sequential linear pr | ogrami | ning, i | Interio | or pe | naity | | |
| Tarreer | on meenod, | externa | | | | | | | | |
| MOD | ULE V | EVOLU | TIONARY OPTIMIZATION TECHNIQUES | | | | | 9 | | |
| Genet | ic algorith | m - wo | rking principle, Basic operators and Terminologies | Build | ing blo | ock h | ypotł | nesis, | | |
| Trave | lling Salesn | nan Prob | em, Particle swam optimization, Ant colony optimization | on. | | | | | | |
| | | | Total | | 45 | нон | PS | | | |
| | | | | | | 1100 | NS | | | |
| REFE | RENCES | | | | | | | | | |
| 1. | David E. G 2009. | oldberg, | Genetic Algorithms in Search, Optimization and Machir | ie Lear | ning, A | ddiso | ו Wes | sley, | | |
| 2. | George J. I | Klir and I | 30 Yuan, Fuzzy Sets and Fuzzy Logic-Theory and Applic | ations, | Prentio | ce Ha | l, 199 | Э5. | | |
| 3. | James A. F Techniques | reeman s, Pearsc | and David M. Skapura, Neural Networks Algorithms, Ap n Edn., 2003. | plicati | ons, an | d Pro | gram | ming | | |
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| P1 | L9VL312 | | F | leconfigurable Arch | itectures | | 3 | 0 | 0 | 3 | |
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| | | CO1 | (Analyz | e) Compare FPGA rou | uting architect | tures | | | | K4 | |
| 0 | utcomes | CO2 | (Unders | stand) Understand th | e application | of FPGA | | | | K2 | |
| | accomes | CO3 | (Under | stand) Understand th | e routina pro | cess in VL | SI desian | | | K2 | |
| | | C04 | (Apply) | Use the concept of H | ligh level synt | hesis. | <u>-</u> | | | K3 | |
| | | CO5 | (Apply) | Design SoC using VH | IDL and Verilo | g HDL co | ding. | | | K3 | |
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| MOD | DULE I | INTRO | DUCTIO | N | | | | | | 9 | |
| of re | s –classificat | systems ion of rec | configura | acteristics of RCS adv ble architecture-fine, | antages and coarse grain & | issues. Fu & hybrid a | indamenta rchitecture | l conce s – Exa | pts & D pts & D pts s | esign | |
| MOD | OULE II | FPGA 1 | ГЕСНNO | LOGIES & ARCHITE | | | | | | 9 | |
| Tech | nology tren | ds- Prog | ramming | technology- SRAM | programmed | FPGAs, | antifuse p | rogram | imed F | - PGAs, | |
| erasa | able progran | nmable l | ogic devi | ces. Alternative FPGA | architectures | <mark>s: M</mark> ux Vs | LUT base | d logic | blocks | - CLB | |
| Vs L/ | AB Vs Slices- | - Fast car | ry chains | - Embedded RAMs- F | PGA <mark>Vs ASIC</mark> | <mark>design s</mark> ty | /les. | | | | |
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SEMESTER II - ELECTIVE IV

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| P19VL313 | CMOS | DIGITAL VLSI DESIGN | 3 | 0 | 0 | 3 | |
| | Upon d | completion of this course, students will be able to | | | | | |
| | CO1 | (Understand) Understand the transistor level design a logic. | and CM | OS inve | rter | K2 | |
| 0 | CO2 | (Apply) Design static and dynamic circuits with the aid | l of des | ign rule | s. | K3 | |
| Outcomes | CO3 | (Apply) Design latches and registers by analyzing timi | ng issu | es. | | K3 | |
| | CO4 (Understand) Understand the design methodology of arithmetic building block | | | | | | |
| | CO5 | (Understand) Understand the interconnect and clocking | ng strat | egies | | K2 | |
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| MODULE I | MOS | RANSISTOR PRINCIPLES AND CMOS INVERTER | | | | 9 | |
| parameters. | ining c | Lendershin & Excellence | Lifergy | , and | Lifergy | Delay | |
| MODULE II | СОМВ | INATIONAL LOGIC CIRCUITS | | | | 9 | |
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| MODULE III | SEQU | | | | 1161 | 9 | |
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| | Upon c | completion of this course, students will be able to | | | | |
| | CO1 | (Analyze) Compare different architecture design | | | | K4 |
| | CO2 | (Inderstand) Understand the different routing algorith | nms | | | K2 |
| Outcomes | CO3 | (Understand) Understand the three dimensional r | network | ks-on-cl | nip | K2 |
| | C04 | (Analyze) Analyze test and fault tolerance of Communi | ications | in NOC | | K4 |
| | C05 | (Apply) Apply the 3D Integration procedures in NOC | cutionic | | - | K3 |
| | | | | | | |
| 10DULE I | INTRO | DDUCTION TO NOC | | | | 9 |
| Introduction to | NoC - | OSI layer rules in NoC - Interconnection Networks in | n Netw | ork-on- | Chip N | letwo |
| Fopologies - Sw | itching Te | echniques - Routing Strategies - Flow Control Protocol Qu | ality-of | -Servic | e Supp | ort |
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| MODULE II | ARCH | ITECTURE DESIGN | | | | 9 |
| Switching Tech | niques ar | nd Packet Format - Asynchronous FIFO Design -GALS | Style | of Con | nmunic | ation |
| Normhole Route | er Archite | cture Design - VC Router Architecture Design - Adaptive F | Router | Archite | cture D | esigr |
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| 10DULE III | ROUT | ING ALGORITHM | | | | 9 |
| Packet routing-(| Qos, cong | jestion control and flow control – rou <mark>ter design</mark> – networ | k link d | lesign - | - Efficie | ent a |
| Deadlock-Free | Free-Base | ed Multicast Routing Methods - Path-Based Multicast Ro | outina 1 | for 2D | and 3D | - NA |
| VIOTWORKS Foult | | | | | |) Me |
| NELWOIKS- FAUL | -Tolerant | Routing Algorithms - Reliable and Adaptive Routing Algor | rithms | | |) Me |
| | -Tolerant | Routing Algorithms - Reliable and Adaptive Routing Algor | rithms | | | |
| MODULE IV | Tolerant | Routing Algorithms - Reliable and Adaptive Routing Algor AND FAULT TOLERANCE OF NOC | rithms | | | Э Ме: 9 |
| MODULE IV Design-Security | Tolerant | Routing Algorithms - Reliable and Adaptive Routing Algor AND FAULT TOLERANCE OF NOC orks-on-Chips-Formal Verification of Communications in I | rithms | ks-on C | chips Te | 9 est a |
| MODULE IV Design-Security Fault Tolerance | Tolerant TEST A in Netwo for Netwo | Routing Algorithms - Reliable and Adaptive Routing Algor AND FAULT TOLERANCE OF NOC orks-on-Chips-Formal Verification of Communications in I orks-on-Chip Infrastructures-Monitoring Services for Netw | nithms Networks-or | ks-on C 1 Chips. | Chips Te | 9 9 est a |
| MODULE IV Design-Security Fault Tolerance | Tolerant TEST | Routing Algorithms - Reliable and Adaptive Routing Algor AND FAULT TOLERANCE OF NOC orks-on-Chips-Formal Verification of Communications in I orks-on-Chip Infrastructures-Monitoring Services for Netw | Network vorks-or | ks-on C 1 Chips. | Chips Te | 9 est ai |
| MODULE IV Design-Security Fault Tolerance | Tolerant TEST A in Netwo for Netwo THREE | Routing Algorithms - Reliable and Adaptive Routing Algor AND FAULT TOLERANCE OF NOC orks-on-Chips-Formal Verification of Communications in I orks-on-Chip Infrastructures-Monitoring Services for Netw E-DIMENSIONAL INTEGRATION OF NETWORK-ON-C | Networks-or | ks-on C n Chips | Chips Te | 9 est ar 9 |
| MODULE IV Design-Security Fault Tolerance MODULE V | TEST A in Netwo for Netwo THREE | Routing Algorithms - Reliable and Adaptive Routing Algor AND FAULT TOLERANCE OF NOC orks-on-Chips-Formal Verification of Communications in I orks-on-Chip Infrastructures-Monitoring Services for Netw E-DIMENSIONAL INTEGRATION OF NETWORK-ON-Ch orks-on-Chips Architectures. – A Novel Dimensionally-Dec | rithms Network orks-or HIP | ks-on C n Chips. ed Rout | chips Te | 9 est ar 9 On- |
| MODULE IV Design-Security Fault Tolerance MODULE V Three-Dimension Chip Communica | TEST A in Netwo for Netwo THREE nal Netwo ation in 3 | Routing Algorithms - Reliable and Adaptive Routing Algor AND FAULT TOLERANCE OF NOC orks-on-Chips-Formal Verification of Communications in I orks-on-Chip Infrastructures-Monitoring Services for Netw E-DIMENSIONAL INTEGRATION OF NETWORK-ON-Cl orks-on-Chips Architectures. – A Novel Dimensionally-Dec D Architectures - Resource Allocation for QoS On-Chip Co | Network orks-or HIP compose | ks-on C n Chips ed Rout cation - | Chips Te eer for (- Netwo | 9 est a 9 On- orks- |
| MODULE IV Design-Security Fault Tolerance MODULE V Ihree-Dimension Chip Communication-Chip Protoco | Tolerant in Netwo for Netwo THREE nal Netwo ation in 3 ls-On-Chi | Routing Algorithms - Reliable and Adaptive Routing Algor AND FAULT TOLERANCE OF NOC orks-on-Chips-Formal Verification of Communications in I orks-on-Chip Infrastructures-Monitoring Services for Network E-DIMENSIONAL INTEGRATION OF NETWORK-ON-CL orks-on-Chips Architectures. – A Novel Dimensionally-Dec D Architectures - Resource Allocation for QoS On-Chip Co ip Processor Traffic Modeling for Networks-on Chip | rithms Network orks-or HIP compose mmuni | ks-on C n Chips. ed Rout cation - | chips Te | 9 est ar 9 On- orks- |
| MODULE IV Design-Security Fault Tolerance MODULE V Fhree-Dimensio Chip Communication Chip Protoco | Tolerant TEST A in Netwo for Netwo THREE nal Netwo ation in 3 Is-On-Chi | Routing Algorithms - Reliable and Adaptive Routing Algor AND FAULT TOLERANCE OF NOC orks-on-Chips-Formal Verification of Communications in I orks-on-Chip Infrastructures-Monitoring Services for Netw E-DIMENSIONAL INTEGRATION OF NETWORK-ON-Cl orks-on-Chips Architectures. – A Novel Dimensionally-Dec D Architectures - Resource Allocation for QoS On-Chip Co ip Processor Traffic Modeling for Networks-on Chip | Networks-or orks-or HIP compose mmuni | ks-on C n Chips. ed Rout cation - | chips Te | 9 est ai 9 On- orks- |
| MODULE IV Design-Security Fault Tolerance MODULE V Fhree-Dimension Chip Communica on-Chip Protoco | Tolerant TEST in Netwo for Netwo THREE nal Netwo ation in 3 Is-On-Chi | Routing Algorithms - Reliable and Adaptive Routing Algor AND FAULT TOLERANCE OF NOC orks-on-Chips-Formal Verification of Communications in I orks-on-Chip Infrastructures-Monitoring Services for Netw E-DIMENSIONAL INTEGRATION OF NETWORK-ON-Cl orks-on-Chips Architectures. – A Novel Dimensionally-Dec D Architectures - Resource Allocation for QoS On-Chip Co ip Processor Traffic Modeling for Networks-on Chip | rithms Network orks-or HIP compose mmuni | ks-on C n Chips ed Rout cation - otal: 4 | chips Te er for (- Netwo 5 HOU | 9 est ai 9 On- orks- RS |
| MODULE IV Design-Security Fault Tolerance MODULE V Three-Dimension Chip Communica on-Chip Protoco | Tolerant in Netwo for Netwo THREE nal Netwo ation in 3 Is-On-Chi | Routing Algorithms - Reliable and Adaptive Routing Algor AND FAULT TOLERANCE OF NOC orks-on-Chips-Formal Verification of Communications in I orks-on-Chip Infrastructures-Monitoring Services for Netw E-DIMENSIONAL INTEGRATION OF NETWORK-ON-Cl orks-on-Chips Architectures. – A Novel Dimensionally-Dec D Architectures - Resource Allocation for QoS On-Chip Co ip Processor Traffic Modeling for Networks-on Chip | rithms Network orks-or HIP compose mmuni | ks-on C n Chips ed Rout cation - otal: 4 | Chips Te er for (- Netwo 5 HOU | 9 est a 9 On- orks- RS |
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| MODULE IV Design-Security Fault Tolerance MODULE V Three-Dimension Chip Communica on-Chip Protoco REFERENCES: 1 Chrysosto Holistic De | Tolerant in Netwo for Netwo THREE nal Netwo ation in 3 Is-On-Chi is-On-Chi | Routing Algorithms - Reliable and Adaptive Routing Algor AND FAULT TOLERANCE OF NOC orks-on-Chips-Formal Verification of Communications in I orks-on-Chip Infrastructures-Monitoring Services for Netw E-DIMENSIONAL INTEGRATION OF NETWORK-ON-Cl orks-on-Chips Architectures. – A Novel Dimensionally-Dec D Architectures - Resource Allocation for QoS On-Chip Co ip Processor Traffic Modeling for Networks-on Chip | vorks-o | ks-on C n Chips ed Rout cation - otal: 4 n-Chip | chips Te er for (- Netwo 5 HOU | 9 est an 9 On- orks- RS ecture |
| MODULE IV Design-Security Fault Tolerance MODULE V Three-Dimension Chip Communication Chip Protoco REFERENCES: 1 Chrysosto Holistic De 2. Fayezgeba CRC press | Tolerant TEST / in Netwo for Netwo THREE nal Netwo ation in 3 Is-On-Chi ation in 3 Is-On-Chi esign Exp ali, Hayth 5. | Routing Algorithms - Reliable and Adaptive Routing Algor AND FAULT TOLERANCE OF NOC orks-on-Chips-Formal Verification of Communications in I orks-on-Chip Infrastructures-Monitoring Services for Netw E-DIMENSIONAL INTEGRATION OF NETWORK-ON-Cl orks-on-Chips Architectures. – A Novel Dimensionally-Dec D Architectures - Resource Allocation for QoS On-Chip Co ip Processor Traffic Modeling for Networks-on Chip opoulos, Vijaykrishnan Narayanan, Chita R.Das, "Netwo loration", Springer. mamelmiligi, Hqhahed Watheq E1-Kharashi "Networks-or | rithms Networl orks-or HIP compose mmuni Tc vorks-o n-Chips | ks-on C n Chips ed Rout cation - otal: 4 n-Chip theory | chips Te er for (- Netwo 5 HOU Archite and p | 9 est an 9 On- orks- RS ecture |
| MODULE IV Design-Security Fault Tolerance MODULE V Three-Dimension Chip Communication con-Chip Protoco REFERENCES: 1 Chrysoston Holistic Data 2. Fayezgeba 3. Konstantin | Tolerant in Netwo for Netwo THREE nal Netwo ation in 3 Is-On-Chi sign Exp ali, Hayth s. nos Tatas | Routing Algorithms - Reliable and Adaptive Routing Algor AND FAULT TOLERANCE OF NOC Drks-on-Chips-Formal Verification of Communications in I Drks-on-Chip Infrastructures-Monitoring Services for Netw E-DIMENSIONAL INTEGRATION OF NETWORK-ON-Cl Drks-on-Chips Architectures. – A Novel Dimensionally-Dec D Architectures - Resource Allocation for QoS On-Chip Co ip Processor Traffic Modeling for Networks-on Chip opoulos, Vijaykrishnan Narayanan, Chita R.Das, "Networks- loration", Springer. hamelmiligi, Hqhahed Watheq E1-Kharashi "Networks-on-Chips and Kostas Siozios "Designing 2D and 3D Network-on-Chips and Kostas Siozios "Designing 2D and 3D Network-on-Chips and Kostas Siozios "Designing 2D and 3D Network-on-Chips D Architectures - Resource 2D And 3D Network-on-Chi | rithms Network orks-or HIP compose mmuni Tc vorks-o n-Chips hip Arch | ks-on C n Chips. ed Rout cation - otal: 4 n-Chip theory | chips Te chips Te er for (- Netwo 5 HOU Archite and p es" 201 | 9 est a 9 On- orks- RS ecture oractio |
| MODULE IV Design-Security Fault Tolerance MODULE V Three-Dimension Chip Communication on-Chip Protoco REFERENCES: 1 Chrysoston Holistic De 2. Fayezgeba 3. Konstantin 4. Palesi, Ma | Tolerant in Netwo for Netwo for Netwo THREE nal Netwo ation in 3 Is-On-Chi Is-On-Chi sign Exp ali, Hayth s. nos Tatas urizio, Da | Routing Algorithms - Reliable and Adaptive Routing Algor AND FAULT TOLERANCE OF NOC orks-on-Chips-Formal Verification of Communications in I orks-on-Chip Infrastructures-Monitoring Services for Netw E-DIMENSIONAL INTEGRATION OF NETWORK-ON-Cl orks-on-Chips Architectures. – A Novel Dimensionally-Dec D Architectures - Resource Allocation for QoS On-Chip Co ip Processor Traffic Modeling for Networks-on Chip opoulos, Vijaykrishnan Narayanan, Chita R.Das, "Netwo loration", Springer. hamelmiligi, Hqhahed Watheq E1-Kharashi "Networks-on-Ch aneshtalab, Masoud "Routing Algorithms in Networks-on-Ch | rithms Network orks-or HIP compose mmuni Tc vorks-o n-Chips hip Arch Chip" 20 | ks-on C n Chips ed Rout cation - otal: 4 n-Chip theory nitectur 014 | chips Te cer for (- Netwo 5 HOU Archite and p es" 201 | 9 est an 9 On- orks- RS ecture oractie |

| D10)/J 21 5 | DECIC | | L | Т | Ρ | С |
|------------------------------------|----------------------|---|-----------------------|------------------|--------|-----------|
| P19VL315 | DESIG | DESIGN AND ANALYSIS OF COMPUTER ALGORITHMS 3 0 0 | | | | |
| | Upon c | completion of this course, students will be able to | | | | |
| | CO1 | (Apply) Apply the suitable algorithm according to the problem. | given o | ptimiza | ation | K3 |
| | CO2 | (Analyze) Modify the algorithms to refine the complex | ity para | meters | 5. | K4 |
| Outcomes | CO3 | (Understand) Understand the various algorithms sorting. | for sea | rching | and | K2 |
| | CO4 | (Apply) Apply the graph algorithms in path of circuits. | | | | K3 |
| | CO5 | (Understand) Understand the parallel algorithe algorithms. | ms an | d Ger | netic | K2 |
| | | | | | | |
| MODULE I | INTRO | DDUCTION | | | | 9 |
| Polynomial and direct / indirect / | Exponen / determi | tial algorithms, big "oh" and small "oh" notation, exa inistic algorithms, static and dynamic complexity, stepwi | ct algor se refine | rithms ement. | and he | uristics, |
| | | 1 1 1 0 0 11 | | | | |

MODULE II DESIGN TECHNIQUES

Subgoals method, working backwards, work tracking, branch and bound algorithms for traveling salesman problem and knapsack problem, hill climbing techniques, divide and conquer method, dynamic programming, greedy methods.

MODULE III SEARCHING AND SORTING

Sequential search, binary search, block search, Fibonacci search, bubble sort, bucket sorting, quick sort, heap sort, average case and worst case behavior

MODULE IV GRAPH ALGORITHMS

Minimum spanning, tree, shortest path algorithms, R-connected graphs, Even's and Kleitman's algorithms, max-flow min cut theorem, Steiglitz's link deficit algorithm.

MODULE V SELECTED TOPICS

NP Completeness Approximation Algorithms, NP Hard Problems, Strasseu's Matrix Multiplication Algorithms, Magic Squares, Introduction To Parallel Algorithms and Genetic Algorithms, Monte-Carlo Methods, Amortised Analysis.

Total:

45 HOURS

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- 1 D.E.Goldberg, "Genetic Algorithms : Search Optimization and Machine Learning", Addison Wesley, 1989.
- 2. E.Horowitz and S.Sahni, "Fundamentals of Computer Algorithms", Galgotia Publications, 1988.
- 3. Sara Baase, "Computer Algorithms : Introduction to Design and Analysis", Addison Wesley, 1988.
- 4. T.H.Cormen, C.E.Leiserson and R.L.Rivest, "Introduction to Algorithms", Mc Graw Hill, 1994.

| D10)// 216 | DICI | AL TMAGE PROCESSING | | Т | Ρ | С |
|------------|--------|--|----------|---------|-----|----|
| P19VL316 | DIGII | AL IMAGE PROCESSING | 3 | 0 | 0 | 3 |
| | Upon c | ompletion of this course, students will be able to | | | | |
| | CO1 | Employ color image processing techniques. | | | | К3 |
| | CO2 | Apply morphological image processing algorithms. | | | | |
| Outcomes | CO3 | Apply segmentation algorithms and descriptors for ima | ge proc | essing. | | К3 |
| | CO4 | Demonstrate knowledge of image acquisition an enhancement | d digiti | zation | for | K2 |
| | CO5 | Apply compression, watermarking and stenograph images. | ny algo | orithms | to | K4 |
| | | | | | | |

MODULE I DIGITAL IMAGE FUNDAMENTALS

A simple image model, Sampling and Quantization, Imaging Geometry, Digital Geometry, Image Acquisition Systems, Different types of digital images. Basic concepts of digital distances, distance transform, medial axis transform, component labeling, thinning, morphological processing, extension to gray scale morphology.

MODULE II IMAGE TRANSFORMS

1D DFT, 2D transforms - DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Wavelet transform.

MODULE III SEGMENTATION OF GRAY LEVEL IMAGES

Histogram of gray level images, multilevel thresholding, Optimal thresholding using Bayesian classification, Watershed and Dam Construction algorithms for segmenting gray level image. Detection of edges and lines: First order and second order edge operators, multi-scale edge detection, Canny's edge detection algorithm, Hough transform for detecting lines and curves, edge linking.

MODULE IV IMAGE ENHANCEMENT AND COLOR IMAGE PROCESSING

Point processing, Spatial Filtering, Frequency domain filtering, multi-spectral image enhancement, image restoration. Color Representation, Laws of color matching, chromaticity diagram, color enhancement, color image segmentation, color edge detection, color demosaicing.

MODULE V IMAGE COMPRESSION

Lossy and lossless compression schemes, prediction based compression schemes, vector quantization, subband encoding schemes, JPEG compression standard, Fractal compression scheme, Wavelet compression scheme.

Total: 45 HOURS

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| REFE | RENCES: |
|------|--|
| 1. | A.K. Jain, "Fundamentals of Digital Image Processing", Prentice-Hall, Addison-Wesley, 1989. |
| 2. | Bovik (ed.), "Handbook of Image and Video Processing", Academic Press, 2000. |
| 3. | B. Jähne, "Practical Handbook on Image Processing for Scientific Applications", CRC Press, 1997. |
| 4. | Bernd Jähne, Digital Image Processing, Springer-Verlag Berlin Heidelberg 2005. |
| 5. | Gonzalez and Woods, Digital Image Processing, Prentice-Hall. |
| 6. | J. C. Russ. The Image Processing Handbook. CRC, Boca Raton, FL, 4th edn., 2002. |
| 7. | J. S. Lim, "Two-dimensional Signal and Image Processing" Prentice-Hall, 1990. |
| 8. | M. Petrou, P. Bosdogianni, "Image Processing, The Fundamentals", Wiley, 1999. |

| SI.No. | Course Code | Course Title | Category | Contact Periods | L | т | Ρ | С |
|--------|----------------|----------------------|----------|--------------------|---|---|----|----|
| THEOR | Y | | | | | | | |
| 1 | P19VL3XX | Program Elective V | PE | 3 | 3 | 0 | 0 | 3 |
| 2 | P19OE4XX | Open Elective | OE | 3 | 3 | 0 | 0 | 3 |
| PRACTI | CALS | | | | | | | |
| 3 | P19VL202 | Project Work Phase I | PW | 16 | 0 | 0 | 16 | 8 |
| | | TOTAL | | 22 | 6 | 0 | 16 | 14 |

Semester III

PROGRAM ELECTIVES (PE)

| SI.No. | Course Code | Course Title | Category | L | Т | Ρ | С |
|--------|----------------|--|----------|---|---|---|---|
| 1 | P19VL317 | MEMS and NEMS | PE | 3 | 0 | 0 | 3 |
| 2 | P19VL318 | Signal Integrity for High Speed Design | PE | 3 | 0 | 0 | 3 |
| 3 | P19VL319 | Nanoscale Devices | PE | 3 | 0 | 0 | 3 |
| 4 | P19VL320 | Scripting Languages for VLSI | PE | 3 | 0 | 0 | 3 |



| D10V/ 217 | MEMO | AND NEMS | L | Т | Ρ | С | | |
|-----------|------|---|-----------|-----------|------|----|--|--|
| F197L31/ | MEMS | S AND NEMS | 3 | 0 | 0 | 3 | | |
| | Upon | completion of this course, students will be able to | | | | | | |
| Outcomes | C01 | (Understand) Understand the operation of micro of and their applications | evices, r | micro sys | tems | K2 | | |
| | C02 | (Apply) Design the micro devices, micro syste fabrication process. | ms usin | ng the N | 1EMS | К3 | | |
| | CO3 | (Apply) Design concepts of micro sensors. | | | | K3 | | |
| | CO4 | (Apply) Design concepts of micro actuators. | | | | K3 | | |
| | CO5 | (Apply) Develop experience on micro/nano systems | for pho | tonics . | | K3 | | |
| | | | | | | | | |

MODULE I OVERVIEW

New trends in Engineering and Science: Micro and Nanoscale systems, Introduction to Design of MEMS and NEMS, MEMS and NEMS – Applications, Devices and structures. Materials for MEMS: Silicon, silicon compounds, polymers, metals.

MODULE II MEMS FABRICATION TECHNOLOGIES

Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect- Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials

MODULE III MICRO SENSORS

MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors- engineering mechanics behind these Microsensors. Case study: Piezo-resistive pressure sensor.

MODULE IV MICRO ACTUATORS

Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces (Parallel plate, Torsion bar, Comb drive actuators), Micromechanical Motors and pumps. Case study: Comb drive actuators.

MODULE V NANOSYSTEMS AND QUANTUM MECHANICS

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation and Wave function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

Total : 45 HOURS

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- 1. Chang Liu, "Foundations of MEMS", Pearson education India limited, 2006.
- 2. Marc Madou, "Fundamentals of Microfabrication", CRC press 1997.
- 3. Stephen D. Senturia," Micro system Design", Kluwer Academic Publishers,2001
- 4. Sergey Edward Lyshevski, "MEMS and NEMS: Systems, Devices, and Structures" CRC Press, 2002.
- 5. Tai Ran Hsu ,"MEMS and Microsystems Design and Manufacture" ,Tata Mcraw Hill, 2002.

| P19VL318 | STON | | L | Т | Ρ | С | | | |
|----------|--------|--|--|---------|---|----|--|--|--|
| | SIGN | AL INTEGRITT FOR HIGH SPEED DESIGN | 3 | 0 | 0 | 3 | | | |
| | Upon o | completion of this course, students will be able to | | | | | | | |
| | CO1 | Identify sources affecting the speed of digital circuits. | lentify sources affecting the speed of digital circuits. | | | | | | |
| | CO2 | Discuss the ways to Improve the signal transmission characteristics. | | | | | | | |
| Outcomes | CO3 | Identify sources affecting the speed of digital circuits. | | | | K2 | | | |
| | CO4 | Introduce methods to improve the signal characteristics | transı | mission | | К2 | | | |
| | CO5 | Discuss about Clock Distribution And Clock Oscillators | | | | K2 | | | |
| | | | | | | | | | |

MODULE ISIGNAL PROPAGATION ON TRANSMISSION LINES9Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic
impedance, wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field
maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu
thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and
terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section,
reflection coefficient, skin-effect, dispersion

MODULE II MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossles models

MODULE III NON-IDEAL EFFECTS

Non-ideal signal return paths – gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses – Rs, tanδ , routing parasitic, Common-mode current, differential-mode current , Connectors

MODULE IV POWER CONSIDERATIONS AND SYSTEM DESIGN

SSN/SSO, DC power bus design, layer stack up, SMT decoupling, Logic families, power consumption, and system power delivery, Logic families and speed Package types and parasitic ,SPICE, IBIS models, Bit streams, PRBS and filtering functions of link-path components, Eye diagrams, jitter, inter-symbol interference Bit-error rate, Timing analysis

MODULE V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

Total : 45 HOURS

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- 1. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall PTR, 2003.
- 2. Eric Bogatin , Signal Integrity Simplified , Prentice Hall PTR, 2003.
- 3. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993.
- 4. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of
- ^{4.} Interconnect Theory and Design Practices, Wiley-Interscience, 2000.

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|-----------|--------------------------------------|--|-----------|--------|----|----|--|
| PISVLSIS | NANOSCALE DEVICES 3 | | | | 0 | 3 | |
| | Upon o | completion of this course, students will be able to | | | | | |
| | CO1 | Interpret novel MOSFET devices and understand the multi-gate devices | ne adva | ntages | of | К2 | |
| Outcomes | CO2 | Discuss the physical insight of their functional characteristics | | | | | |
| | CO3 | Interpret Nanowire Fets And Transistors At The Molecu | ılar Scal | e | | K2 | |
| | CO4 Explain the effects of Radiation | | | | | | |
| | CO5 | Design of circuits using Multigate Devices | | | | K3 | |
| | | | | | | | |

MODULE IINTRODUCTION TO NOVEL MOSFETS9MOSFET scaling, short channel effects - channel engineering - source/drain engineering - high k dielectric -
copper interconnects - strain engineering, SOI MOSFET, multigate transistors - single gate - double gate -
triple gate - surround gate, quantum effects - volume inversion - mobility - threshold voltage - inter
subband scattering, multigate technology - mobility - gate stack9

MODULE II PHYSICS OF MULTIGATE MOS SYSTEMS

MOS Electrostatics – 1D – 2D MOS Electrostatics, MOSFET Current-Voltage Characteristics – CMOS Technology – Ultimate limits, double gate MOS system – gate voltage effect - semiconductor thickness effect – asymmetry effect – oxide thickness effect – electron tunnel current – two dimensional confinement, scattering – mobility

MODULE III NANOWIRE FETS AND TRANSISTORS AT THE MOLECULAR SCALE

Silicon nanowire MOSFETs – Evaluvation of I-V characteristics – The I-V characteristics for non-degenerate carrier statistics – The I-V characteristics for degenerate carrier statistics – Carbon nanotube – Band structure of graphene – Physical structure of nanotube – Band structure of nanotube – Carbon nanotube FETs – Carbon nanotube MOSFETs – Schottky barrier carbon nanotube FETs – Electronic conduction in molecules – General model for ballistic nano transistors – MOSFETs with 0D, 1D, and 2D channels – Molecular transistors – Single electron charging – Single electron transistors

MODULE IV RADIATION EFFECTS

Radiation effects in SOI MOSFETs, total ionizing dose effects – single gate SOI – multigate devices, single event effect, scaling effects

MODULE V CIRCUIT DESIGN USING MULTIGATE DEVICES

Digital circuits – impact of device performance on digital circuits – leakage performance trade off – multi VT devices and circuits – SRAM design, analog circuit design – transconductance - intrinsic gain – flicker noise – self heating –band gap voltage reference – operational amplifier – comparator designs, mixed signal – successive approximation DAC, RF circuits.

Total : 45 HOURS

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g

- 1. J P Colinge, "FINFETs and other multi-gate transistors", Springer Series on integrated circuits and systems, 2008
- Mark Lundstrom, Jing Guo, "Nanoscale Transistors: Device Physics, Modeling and Simulation", Springer, 2006
- 3. M S Lundstorm, "Fundamentals of Carrier Transport", 2nd Ed., Cambridge University Press, Cambridge UK, 2000

| D10// 320 | | | L | Т | Р | С | | |
|-----------|--|--|------|---|---|----|--|--|
| F 1976520 | SCRIPTING LANGUAGES FOR VEST | | | 0 | 0 | 3 | | |
| | Upon completion of this course, students will be able to | | | | | | | |
| | CO1 | (Understand) Understand the basics of SCRIPTING and PERL | | | | K2 | | |
| Outcomes | CO2 | (Analyze) Interpret advanced PERL | | | | K4 | | |
| outcomes | CO3 | (Understand) Understand the concept of TCL phenon | nena | | | K2 | | |
| | CO4 | (Analyze) Interpret advanced TCL | | | | K4 | | |
| | CO5 | (Apply) Create Tool Kit and Java script | | | | K3 | | |
| | | | | | | | | |

MODULE I INTRODUCTION TO SCRIPTING AND PERL

Characteristics of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

MODULE II ADVANCED PERL

Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

MODULE III TCL

The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

MODULE IV ADVANCED TCL

The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running un trusted code, The C interface.

MODULE V TK AND JAVA SCRIPT

Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK. JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Python. Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

Total : 45 HOURS

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- 1. Brent Welch, "Practical Programming in Tcl and Tk", Fourth Edition, 2003.
- 2. David Barron, "The World of Scripting Languages", Wiley Publications, 2000.
- 3. Guido van Rossum, and Fred L. Drake ", Python Tutorial, Jr., editor, Release 2.6.4
- 4. Randal L. Schwartz, "Learning PERL", Sixth Edition, O"Reilly.

| SI.No. | Course Code | Course Title | Category | L | Т | Ρ | С |
|--------|----------------|---------------------|----------|---|---|---|---|
| 1 | P190E401 | Business Analytics | OE | 3 | 0 | 0 | 3 |
| 2 | P190E402 | Industrial Safety | OE | 3 | 0 | 0 | 3 |
| 3 | P19OE403 | Operations Research | OE | 3 | 0 | 0 | 3 |
| 5 | P190E404 | Composite Materials | OE | 3 | 0 | 0 | 3 |

OPEN ELECTIVES



| D100E401 | DUCTA | | L | Т | Р | С | | | | | |
|--|--------------------|--|----------|----------|--------|----------|--|--|--|--|--|
| P190E401 | BUSINESS ANALYTICS | | | 0 | 0 | 3 | | | | | |
| Upon completion of this course, students will be able to | | | | | | | | | | | |
| | CO1 | (Apply) Identify the real world business problems and model with analytical solutions. | | | | | | | | | |
| Outcomos | CO2 | (Analyze) Solve analytical problem with relevent background knowledge | vant r | mathem | atics | K4 | | | | | |
| Outcomes | CO3 | (Apply) Convert any real world decision making problem to hypothesis and apply suitable statistical testing | | | | | | | | | |
| | CO4 | (Apply) Use open source frameworks for modeling and storing data. | | | | | | | | | |
| | CO5 | (Apply) Apply suitable visualization technique using voluminous data | g R fo | r visual | izing | K3 | | | | | |
| | | | | | | | | | | | |
| MODULE I | OVER | VIEW OF BUSINESS ANALYTICS | | | | 9 | | | | | |
| Introduction – D | Drivers f | or Business Analytics – Applications of Business Ana | lytics: | Marketiı | ng and | Sales, | | | | | |
| Human Resource | e, Healt | hcare, Product Design, Service Design, Customer Se | ervice a | and Sup | port - | - Skills | | | | | |

Required for a Business Analyst – Framework for Business Analytics Life Cycle for Business Analytics Process.

MODULE II ESSENTIALS OF BUSINESS ANALYTICS

Descriptive Statistics - Using Data - Types of Data - Data Distribution Metrics: Frequency, Mean, Median, Mode, Range, Variance, Standard Deviation, Percentile, Quartile, z-Score, Covariance, Correlation - Data Visualization: Tables, Charts, Line Charts, Bar and Column Chart, Bubble Chart, Heat Map - Data Dashboards.

MODELING UNCERTAINTY AND STATISTICAL INFERENCE MODULE III

Modeling Uncertainty: Events and Probabilities – Conditional Probability – Random Variables – Discrete Probability Distributions – Continuous Probability Distribution – Statistical Inference: Data Sampling – Selecting a Sample – Point Estimation – Sampling Distributions – Interval Estimation – Hypothesis Testing.

MODULE IV ANALYTICS USING HADOOP AND MAPREDUCE FRAMEWORK

Introducing Hadoop – RDBMS versus Hadoop – Hadoop Overview – HDFS (Hadoop Distributed File System) - Processing Data with Hadoop - Introduction to MapReduce - Features of MapReduce – Algorithms Using Map-Reduce: Matrix-Vector Multiplication, Relational Algebra Operations, Grouping and Aggregation – Extensions to MapReduce.

MODULE V **OTHER DATA ANALYTICAL FRAMEWORKS**

Overview of Application development Languages for Hadoop – PigLatin – Hive – Hive Query Language (HQL) – Introduction to Pentaho, JAQL - Introduction to Apache: Sqoop, Drill and Spark, Cloudera Impala -Introduction to NoSQL Databases – Hbase and MongoDB.

Total: 45 HOURS

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REFERENCES:

- 1. VigneshPrajapati, "Big Data Analytics with R and Hadoop", Packt Publishing, 2013.
- AnandRajaraman, Jeffrey David Ullman, "Mining of Massive Datasets", Cambridge University Press, 2. 2012.
- Jeffrey D. Camm, James J. Cochran, Michael J. Fry, Jeffrey W. Ohlmann, David R. Anderson, "Essentials 3. of Business Analytics", Cengage Learning, second Edition, 2016
- U. Dinesh Kumar, "Business Analytics: The Science of Data-Driven Decision Making", Wiley, 2017. 4.
- 5. A. Ohri, "R for Business Analytics", Springer, 2012

Umesh R Hodeghatta, UmeshaNayak, "Business Analytics Using R – A Practical Approach", Apress, 2017 6.

7. Rui Miguel Forte, "Mastering Predictive Analytics with R", Packt Publication, 2015.

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| P190F402 | INDUSTRIAL SAFETY | | | Т | Ρ | С | | | | |
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| | | | | 0 | 0 | 3 | | | | |
| | Upon o | completion of this course, students will be able to | mpletion of this course, students will be able to | | | | | | | |
| | CO1 | (Understand) Get exposed to safety concepts and inc | lustry h | azards | | K2 | | | | |
| Outcomes | CO2 | (Understand) Understand the chemical hazards | | | | K2 | | | | |
| Outcomes | CO3 | (Analyze) Analyze the noise pollution using instrumer | nts | | | K4 | | | | |
| | CO4 | (Analyze) Analyze the hazards using different technic | lues | | | K4 | | | | |
| | CO5 | (Apply) Apply the regulations for safety and control o | f hazard | s | | K3 | | | | |
| | | | | | | | | | | |

MODULE I INTRODUCTION

Evolution of modern safety concepts – Fire prevention – Mechanical hazards – Boilers, Pressure vessels, Electrical Exposure.

MODULE II CHEMICAL HAZARDS

Chemical exposure – Toxic materials – Ionizing Radiation and Non-ionizing Radiation - Industrial Hygiene – Industrial Toxicology.

MODULE III ENVIRONMENTAL CONTROL

Industrial Health Hazards – Environmental Control – Industrial Noise - Noise measuring instruments, Control of Noise, Vibration, - Personal Protection.

MODULE IV HAZARD ANALYSIS

System Safety Analysis –Techniques – Fault Tree Analysis (FTA), Failure Modes and Effects Analysis (FMEA), HAZOP analysis and Risk Assessment

MODULE V SAFETY REGULATIONS

Explosions – Disaster management – catastrophe control, hazard control ,Safety education and training -Factories Act, Safety regulations Product safety – case studies.

Total : 45 HOURS

REFERENCES:

1. John V.Grimaldi, "Safety Management", AITB S Publishers, 2003.

- 2. Safety Manual, "EDEL Engineering Consultancy", 2000.
- 3. David L.Goetsch, "Occupational Safety and Health for Technologists", 5th Edition, Engineers and Managers, Pearson Education Ltd., 2005

| P190E403 | ODED | | L | т | Р | С |
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| | OPERA | ATIONS RESEARCH | 3 | 0 | 0 | 3 |
| | Upon o | completion of this course, students will be able to | | | | |
| | | | | | | |
| | CO1 | (Understand) Understand basics of operation optimization problems | resea | rch an | d | К2 |
| Outcomes | CO2 | (Apply) Apply transportation and network models | | | | K3 |
| | CO3 | (Understand) Understand inventory control models | | | | K2 |
| | CO4 | (Analyze) Analyze the Queuing systems and models | | | | K4 |
| | CO5 | (Apply) Apply decision models for optimization problem | ns | | | К3 |
| | | | | | | |

MODULE I OPERATIONS RESEARCH

The phase of an operation research study – Linear programming – Graphical method– Simplex algorithm – Duality formulation – Sensitivity analysis.

MODULE II TRANSPORTATION MODELS AND NETWORK MODELS

Transportation Assignment Models – Traveling Salesman problem-Networks models – Shortest route – Minimal spanning tree – Maximum flow models – Project network – CPM and PERT networks – Critical path scheduling – Sequencing models

MODULE III INVENTORY MODELS

Inventory models – Economic order quantity models – Quantity discount models – Stochastic inventory models – Multi product models – Inventory control models in practice.

MODULE IV QUEUEING MODELS

Queuing models - Queuing systems and structures – Notation parameter – Single server and multi-server models – Poisson input – Exponential service – Constant rate service – Infinite population – Simulation.

MODULE V DECISION MODELS

Decision models – Game theory – Two person zero sum games – Graphical solution- Algebraic solution- Linear Programming solution – Replacement models – Models based on service life – Economic life– Single / Multi variability search technique – Dynamic Programming – Simple Problem.

Total : 45 HOURS

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- 1. Hillier and Libeberman, "Operations Research", Holden Day, 2005
- 2. Taha H.A., "Operations Research", Sixth Edition, Prentice Hall of India, 2003.
- 3. Bazara M.J., Jarvis and Sherali H., "Linear Programming and Network Flows", John Wiley, 2009.
- 4. Budnick F.S., "Principles of Operations Research for Management", Richard D Irwin, 1990.
- 5. Philip D.T. and Ravindran A., "Operations Research", John Wiley, 1992.
- 6. Shennoy G.V. and Srivastava U.K., "Operation Research for Management", Wiley Eastern, 1994.
- 7. Tulsian and Pasdey V., "Quantitative Techniques", Pearson Asia, 2002.

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Total: 45 HOURS

| D100E40E | | COMD | OSITE MATEDIALS | L | Т | Р | С |
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| F 1902405 | 105 | COMPOSITE MATERIALS | | | 0 | 0 | 3 |
| | | Upon c | completion of this course, students will be able to | | | | |
| Outcomes | | C01 | (Understand) Summarize the various types of Fibe manufacturing methods for Composite materials | ers, Equ | ations | and | K2 |
| | nes | CO2 | (Apply) Derive Flat plate Laminate equations | | | | K3 |
| | | CO3 | (Analyze) Analyze Lamina strength | | | | K4 |
| | | CO4 (Analyze) Analyze the thermal behavior of Composite laminates | | | | | |
| | | CO5 | (Analyze) Analyze Laminate flat plates | | | | K4 |
| | | | | | | | |
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MODULE I INTRODUCTION, LAMINA CONSTITUTIVE EQUATIONS & MANUFACTURING

Definition –Need – General Characteristics, Applications. Fibers – Glass, Carbon, Ceramic and Aramid fibers. Matrices – Polymer, Graphite, Ceramic and Metal Matrices – Characteristics of fibers and matrices. Lamina Constitutive Equations: Lamina Assumptions – Macroscopic Viewpoint. Generalized Hooke's Law. Reduction to Homogeneous Orthotropic Lamina – Isotropic limit case, Orthotropic Stiffness matrix (Qij), Typical Commercial material properties, Rule of Mixtures. Generally Orthotropic Lamina –Transformation Matrix, Transformed Stiffness. Manufacturing: Bag Moulding Compression Moulding – Pultrusion – Filament Winding – Other Manufacturing Processes

MODULE II FLAT PLATE LAMINATE CONSTITUTE EQUATIONS

Definition of stress and Moment Resultants. Strain Displacement relations. Basic Assumptions of Laminated anisotropic plates. Laminate Constitutive Equations – Coupling Interactions, Balanced Laminates, Symmetric Laminates, Angle Ply Laminates, Cross Ply Laminates. Laminate Structural Moduli. Evaluation of Lamina Properties from Laminate Tests. Quasi-Isotropic Laminates. Determination of Lamina stresses within Laminates.

MODULE III LAMINA STRENGTH ANALYSIS

Introduction - Maximum Stress and Strain Criteria. Von-Misses Yield criterion for Isotropic Materials. Generalized Hill's Criterion for Anisotropic materials. Tsai-Hill's Failure Criterion for Composites. Tensor Polynomial (Tsai-Wu) Failure criterion. Prediction of laminate Failure.

MODULE IV THERMAL ANALYSIS

Assumption of Constant C.T.E's. Modification of Hooke's Law. Modification of Laminate Constitutive Equations. Orthotropic Lamina C.T.E's. C.T.E's for special Laminate Configurations – Unidirectional, Off-axis, Symmetric Balanced Laminates, Zero C.T.E laminates, Thermally QuasiIsotropic Laminates

MODULE V ANALYSIS OF LAMINATED FLAT PLATES

Equilibrium Equations of Motion - Energy Formulations - Static Bending Analysis - Buckling Analysis- Free Vibrations – Natural Frequencies.

- 1. Gibson, R.F., "Principles of Composite Material Mechanics", Second Edition, McGraw-Hill, CRC press in progress, 1994,
- 2. Hyer, M.W., "Stress Analysis of Fiber Reinforced Composite Materials", McGraw Hill, 1998
- 3. Agarwal, B.D., and Broutman L.J., "Analysis and Performance of Fiber Composites", John Wiley and Sons, New York, 1990.
- 4. Halpin, J.C., "Primer on Composite Materials, Analysis", Technomic Publishing Co., 1984
- 5. Issac M. Daniel and OriIshai, "Engineering Mechanics of Composite Materials", Oxford University Press-2006, First Indian Edition - 2007
- 6. Mallick, P.K., Fiber, "Reinforced Composites: Materials, Manufacturing and Design", Maneel Dekker Inc, 1993.

