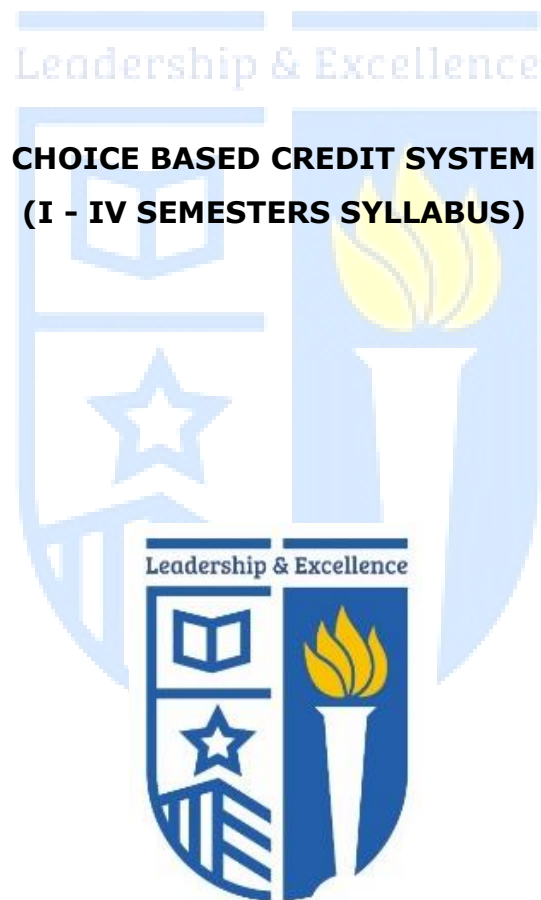


**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.E. VLSI DESIGN**

**Regulation 2019**



**Sri Eshwar College of Engineering**

(An Autonomous Institution)

(Approved by AICTE, Affiliated to Anna University, Chennai)

Kondampatti (Post), Kinathukadavu,

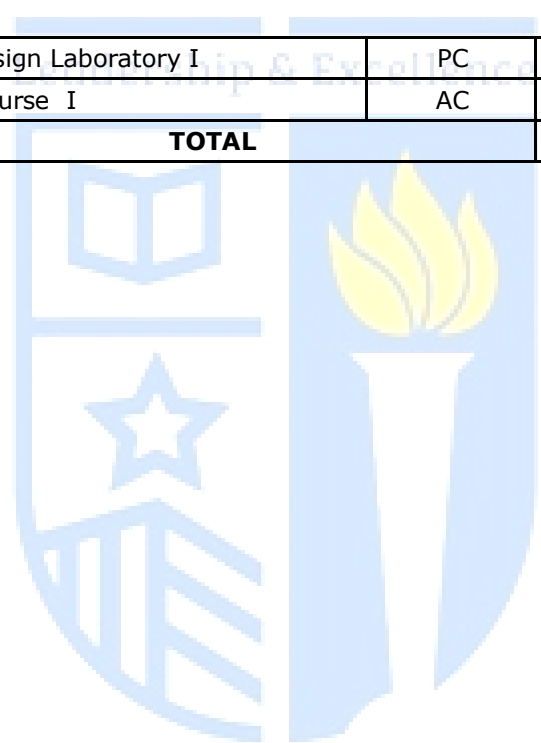
Coimbatore - 641202.

**M.E. VLSI Design**

Regulation 2019

**Semester I**

Sl.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
<b>THEORY</b>								
1	P19MA103	Applied Mathematics for Electronics Engineers	FC	5	3	2	0	4
2	P19VL101	Advanced Digital System Design	PC	3	3	0	0	3
3	P19VL102	CMOS Digital VLSI Design	PC	3	3	0	0	3
4	P19VLXXX	Program Elective I	PE	3	3	0	0	3
5	P19VLXXX	Program Elective II	PE	3	3	0	0	3
6	P19ED102	Research Methodology and IPR	MC	2	2	0	0	2
<b>PRACTICALS</b>								
7	P19VL111	VLSI Design Laboratory I	PC	4	0	0	4	2
8	P19AC5XX	Audit Course I	AC	2	2	0	0	NC
<b>TOTAL</b>				<b>25</b>	<b>19</b>	<b>2</b>	<b>4</b>	<b>20</b>



P19MA103	APPLIED MATHEMATICS FOR COMMUNICATION ENGINEERING	L	T	P	C
		4	0	0	4

After completion of this course, students will be able to

Outcomes		
CO1	( <b>Apply</b> ) Concepts of fuzzy sets, knowledge representation using fuzzy logics, propositions and applications.	K3
CO2	( <b>Apply</b> ) Apply different techniques in matrix theory to solve linear system of equations.	K3
CO3	( <b>Analyze</b> ) Test the nature of linear transformations and analyze the consistency of solutions of linear programming problem.	K4
CO4	( <b>Apply</b> ) Apply the principles of optimality, formulation and computational procedure of dynamic programming.	K3
CO5	( <b>Analyze</b> ) Examine the basic concepts of queuing theory and acquire skills in various queuing models.	K4

### MODULE I FUZZY LOGIC 12

Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.

### MODULE II MATRIX THEORY 12

Cholesky decomposition - Generalized eigenvectors - Canonical basis - QR factorization - Least squares method - Singular value decomposition.

### MODULE III LINEAR PROGRAMMING 12

Formulation of linear programming problem – Graphical solution – Simplex method – Dual simplex method.

### MODULE IV DYNAMIC PROGRAMMING 12

Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of dimensionality.

### MODULE V QUEUEING THEORY 12

Markovian models – Birth and death process. Steady state results: Single and multiple server queueing models - Little's formula.

**TOTAL: 60 Hours**

#### TEXT BOOKS:

- 1 Taha H. A., "Operations Research: An Introduction", 9<sup>th</sup> Edition, Pearson Education, Asia, New Delhi, 2016.
- 2 Bronson R., "Matrix Operations", Schaum's Outline Series, 2<sup>nd</sup> Edition, McGraw Hill, 2011.
- 3 George J. Klir and Yuan, B., "Fuzzy sets and Fuzzy logic, Theory and Applications", Prentice Hall of India Pvt. Ltd., 1997.

#### REFERENCES:

- 1 Johnson R. A., Miller, I and Freund J., "Miller and Freund's Probability and Statistics for Engineers", 8<sup>th</sup> Edition, Pearson Education, Asia, 2015.
- 2 Gross D., Shortle J. F., Thompson J. M and Harris C. M., "Fundamentals of Queueing Theory", 4<sup>th</sup> Edition, John Wiley, 2014.

<b>P19VL101</b>	<b>ADVANCED DIGITAL SYSTEM DESIGN</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>
	Upon completion of this course, students will be able to				
<b>Outcomes</b>	CO1	<b>(Create)</b> Design sequential circuit design.		K6	M1,M2
	CO2	<b>(Analyze)</b> Analyze sequential digital circuits.		K4	M1,M2
	CO3	<b>(Analyze)</b> Analyze the fault diagnosis algorithms and test generation schemes.		K4	M3
	CO4	<b>(Analyze)</b> Analyze sequential circuits and design synchronous design using programmable devices.		K4	M1,M4
	CO5	<b>(Create)</b> Design digital circuits utilizing various constructs of Verilog.		K6	M5

**MODULE I SEQUENTIAL CIRCUIT DESIGN 9**

Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits-ASM chart and realization using ASM

**MODULE II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9**

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

**MODULE III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9**

Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test

**MODULE IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9**

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000

**MODULE V SYSTEM DESIGN USING VERILOG 9**

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modeling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor

**Total : 45 HOURS**

**REFERENCES:**

1. Charles H.Roth Jr "Fundamentals of Logic Design" Thomson Learning 2004
2. M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999
3. M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.
4. Nripendra N Biswas "Logic Design Theory" Prentice Hall of India,2001
5. Parag K.Lala "Fault Tolerant and Fault Testable Hardware Design" B S Publications,2002
6. Parag K.Lala "Digital system Design using PLD" B S Publications,2003
7. S. Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.

P19VL102	CMOS DIGITAL VLSI DESIGN	L	T	P	C
		3	0	0	3

Upon completion of this course, students will be able to

Outcomes			
CO1	<b>(Analyze)</b> Analyze the performance of CMOS Inverter circuits on the basis of their operation and working.	K4	M1
CO2	<b>(Create)</b> Design Combinational logic circuits and sequential logic circuits.	K6	M2,M3
CO3	<b>(Analyze)</b> Discriminate between combinational and sequential circuits.	K4	M2,M3
CO4	<b>(Analyze)</b> Analyze tradeoffs of the various circuit choices for each of the building block.	K4	M4
CO5	<b>(Create)</b> Discuss design methodology of arithmetic building block.	K6	M4,M5

**MODULE I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 9**

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, Technology Scaling - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters.

**MODULE II COMBINATIONAL LOGIC CIRCUITS 9**

Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

**MODULE III SEQUENTIAL LOGIC CIRCUITS 9**

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pulse and sense amplifier based Registers, Non bistable Sequential Circuits.

**MODULE IV ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES 9**

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

**MODULE V INTERCONNECT AND CLOCKING STRATEGIES 9**

Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Self-Timed Circuit Design.

**Total: 45 HOURS**

**REFERENCES:**

1. Jan Rabaey, Anantha Chandrakasan, B Nikolic, "Digital Integrated Circuits: A Design Perspective". Second Edition, Feb 2003, Prentice Hall of India.
2. Jacob Baker "CMOS: Circuit Design, Layout, and Simulation, Third Edition", Wiley IEEE Press 2010 3rd Edition.
3. M J Smith, "Application Specific Integrated Circuits", Addison Wesley, 1997
4. N.Weste, K. Eshraghian, " Principles of CMOS VLSI Design". Second Edition, 1993 Addison Wesley.

P19ED102	RESEARCH METHODOLOGY AND IPR	L	T	P	C
		3	1	0	4
<b>Outcomes</b>	Upon completion of this course, students will be able to				
	CO1	<b>(Analyze)</b> Formulate research problem			K4
	CO2	<b>(Analyze)</b> Carry out research analysis			K4
	CO3	<b>(Analyze)</b> Follow research ethics			K4
		<b>(Understand)</b> Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity			K2
	<b>(Understand)</b> Understand about IPR and filing patents in R & D.			K2	
<b>MODULE I</b>	<b>RESEARCH PROBLEM FORMULATION</b>				<b>9</b>
Meaning of research problem- Sources of research problem, criteria characteristics of a good research problem, errors in selecting a research problem, scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, necessary instrumentations					
<b>MODULE II</b>	<b>LITERATURE REVIEW</b>				<b>9</b>
Effective literature studies approaches, analysis, plagiarism, and research ethics.					
<b>MODULE III</b>	<b>TECHNICAL WRITING /PRESENTATION</b>				<b>9</b>
Effective technical writing, how to write report, paper, developing a research proposal, format of research proposal, a presentation and assessment by a review committee.					
<b>MODULE IV</b>	<b>INTRODUCTION TO INTELLECTUAL PROPERTY RIGHTS (IPR)</b>				<b>9</b>
Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.					
<b>MODULE V</b>	<b>INTELLECTUAL PROPERTY RIGHTS (IPR)</b>				<b>9</b>
Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System, IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.					
					<b>TOTAL: 45 HOURS</b>
<b>REFERENCES:</b>					
1	Asimov, "Introduction to Design", Prentice Hall, 1962.				
2	Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.				
3	Mayall, "Industrial Design", McGraw Hill, 1992.				
4	Niebel, "Product Design", McGraw Hill, 1974.				
5	Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners" 2010				

P19VL111	VLSI Design Laboratory -I	L	T	P	C
		0	0	4	2

Upon completion of this course, students will be able to

Outcomes		
CO1	<b>(Apply)</b> Apply the FPGA platform and carry out a series of validations design.	K3
CO2	<b>(Create)</b> Design and carry out time domain simulations of simple analog building blocks.	K6
CO3	<b>(Create)</b> Design and carry out frequency domain simulations of simple analog building blocks.	K6
CO4	<b>(Evaluate)</b> Evaluate the the pole zero behaviors of feedback based circuits.	K5
CO5	<b>(Create)</b> Design and compute the input/output impedances.	K6

#### List of Experiments

1. Understanding Synthesis principles. Back annotation.
2. Test vector generation and timing analysis of sequential and combinational logic design realized using HDL languages.
3. FPGA real time programming and I/O interfacing.
4. Interfacing with Memory modules in FPGA Boards.
5. Verification of design functionality implemented in FPGA by capturing the signal in DSO.
6. Real time application development.
7. Design Entry Using VHDL or Verilog examples for Digital circuit descriptions using HDL languages sequential, concurrent statements and structural description.

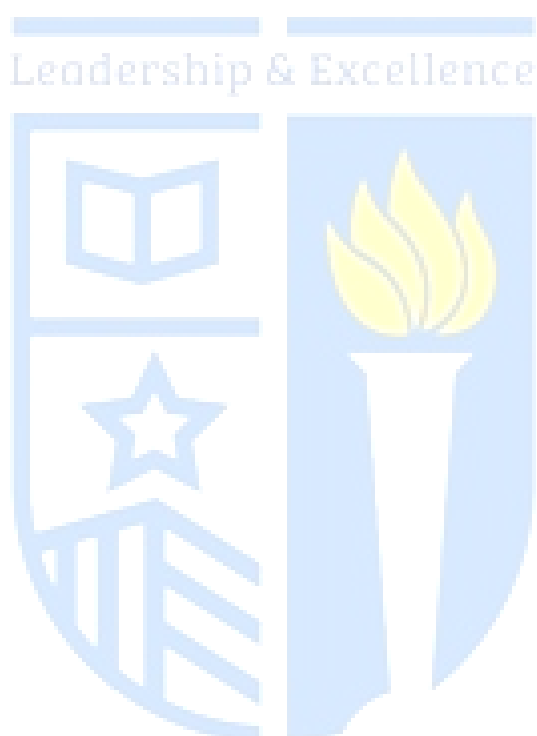
**Total: 45 HOURS**

#### REFERENCES

1. Ming-Bo Lin, Digital System Designs and Practices using Verilog HDL and FPGAs, Wiley, 2012.
2. Samir Palnitkar, Verilog HDL, Pearson Education, 2ndEdition, 2004.
3. J.Bhaskar, A VHDL Primer, Prentice Hall, 1998.
4. M.H.Rashid, Spice for Circuits and Electronics using Pspice, PHI 1995.
5. M.J.S.Smith, Application Specific Integrated Circuits, Pearson Education, 2008.

**PROGRAM ELECTIVES (PE)**

Sl.No	Course Code	Course Title	Course Category	L	T	P	C
<b>SEMESTER I – ELECTIVE I</b>							
1	P19VL301	Device Modeling	PE	3	0	0	3
2	P19VL302	RF IC Design	PE	3	0	0	3
3	P19VL303	Design of Analog Filters and Signal Conditioning Circuits	PE	3	0	0	3
4	P19VL304	CAD for VLSI Circuits	PE	3	0	0	3
<b>SEMESTER I – ELECTIVE II</b>							
5	P19VL305	Embedded System Design	PE	3	0	0	3
6	P19VL306	Advanced Microprocessors and Architectures	PE	3	0	0	3
7	P19VL307	DSP Processor Architecture and Programming	PE	3	0	0	3
8	P19VL308	Digital Control Engineering	PE	3	0	0	3





**SEMESTER I – ELECTIVE I**

		<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>P19VL301</b>	<b>DEVICE MODELING</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

<b>Outcomes</b>				
CO1	<b>(Design)</b> Design MOSFET and BJT devices to desired specifications.		K6	M1-M5
CO2	<b>(Design)</b> Model MOSFET and BJT devices to desired specifications.		K6	M1-M5
CO3	<b>(Analyze)</b> Analyze the CMOS Parameters and performance.		K4	M3
CO4	<b>(Apply)</b> Apply the mathematical techniques for device simulations		K3	M1-M5
CO5	<b>(Analyze)</b> Analyze concepts about Bipolar Devices.		K4	M5

**MODULE I MOS CAPACITORS 9**

Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in an MOS Structure, Polysilicon-Gate Work Function and Depletion Effects, MOS under Nonequilibrium and Gated Diodes, Charge in Silicon Dioxide and at the Silicon-Oxide Interface, Effect of Interface Traps and Oxide Charge on Device Characteristics, High-Field Effects, Impact Ionization and Avalanche Breakdown, Band-to-Band Tunneling, Tunneling into and through Silicon Dioxide, Injection of Hot Carriers from Silicon into Silicon Dioxide, High-Field Effects in Gated Diodes, Dielectric Breakdown

**MODULE II MOSFET DEVICES 9**

Long-Channel MOSFETs, Drain-Current Model, MOSFET I-V Characteristics, Subthreshold Characteristics, Substrate Bias and Temperature Dependence of Threshold Voltage, MOSFET Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, Short-Channel MOSFETs, Short-Channel Effect, Velocity Saturation and High-Field Transport Channel Length Modulation, Source-Drain Series Resistance, MOSFET Degradation and Breakdown at High Fields

**MODULE III CMOS DEVICE DESIGN 9**

MOSFET Scaling, Constant-Field Scaling, Generalized Scaling, Nonscaling Effects, Threshold Voltage, Threshold-Voltage Requirement, Channel Profile Design, Nonuniform Doping, Quantum Effect on Threshold Voltage, Discrete Dopant Effects on Threshold Voltage, MOSFET Channel Length, Various Definitions of Channel Length, Extraction of the Effective Channel Length, Physical Meaning of Effective Channel Length, Extraction of Channel Length by C-V Measurements

**MODULE IV CMOS PERFORMANCE FACTORS 9**

Basic CMOS Circuit Elements, CMOS Inverters, CMOS NAND and NOR Gates, Inverter and NAND Layouts, Parasitic Elements, Source-Drain Resistance, Parasitic Capacitances, Gate Resistance, Interconnect R and C, Sensitivity of CMOS Delay to Device Parameters, Propagation Delay and Delay Equation, Delay Sensitivity to Channel Width, Length, and Gate Oxide Thickness, Sensitivity of Delay to Power-Supply Voltage and Threshold Voltage, Sensitivity of Delay to Parasitic Resistance and Capacitance, Delay of Two-Way NAND and Body Effect, Performance Factors of Advanced CMOS Devices, MOSFETs in RF Circuits, Effect of Transport Parameters on CMOS Performance, Low-Temperature CMOS

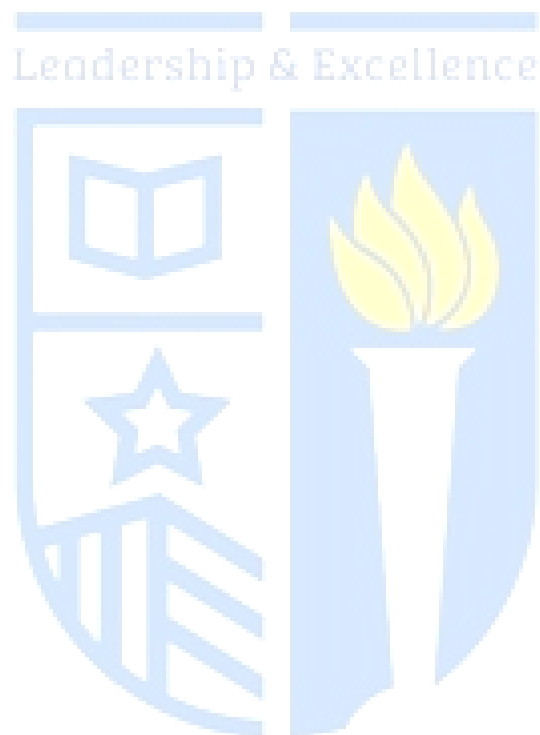
**MODULE V BIPOLAR DEVICES 9**

n-p-n Transistors, Basic Operation of a Bipolar Transistor, Modifying the Simple Diode Theory for Describing Bipolar Transistors, Ideal Current-Voltage Characteristics, Collector Current, Base Current, Current Gains, Ideal IC-VCE Characteristics, Characteristics of a Typical n-p-n Transistor, Effect of Emitter and Base Series Resistances, Effect of Base-Collector Voltage on Collector Current, Collector Current Falloff at High Currents, Nonideal Base Current at Low Currents, Bipolar Device Models for Circuit and Time-Dependent Analyses Basic dc Model, Basic ac Model, Small-Signal Equivalent-Circuit Model, Emitter Diffusion Capacitance, Charge-Control Analysis, Breakdown Voltages, Common-Base Current Gain in the Presence of Base-Collector Junction Avalanche, Saturation Currents in a Transistor, Relation Between BVCEO and BVCEO.

**Total: 45 HOURS**

## REFERENCES

1. Behzad Razavi, "Fundamentals of Microelectronics" Wiley Student Edition, 2nd Edition.
2. J P Collinge, C A Collinge, "Physics of Semiconductor devices" Springer 2002 Edition.
3. Yuan Taur and Tak H. Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, Second Edition.



		<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>P19VL302</b>	<b>RF IC Design</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

<b>Outcomes</b>	CO1	<b>(Understand)</b> Understand the principles of operation of an RF receiver front end	K2	M1-M5
	CO2	<b>(Design)</b> Design the constraints for LNAs, Mixers and Frequency synthesizers	K6	M1-M5
	CO3	<b>(Apply)</b> Apply the constraints for LNAs, Mixers and Frequency synthesizers	K3	M1-M5
	CO4	<b>(Analyze)</b> Analyze the oscillator and sources of noise.	K4	M4
	CO5	<b>(Analyze)</b> Analyze the PLL and frequency Synthesizers.	K6	M5

**MODULE I IMPEDANCE MATCHING IN AMPLIFIERS 9**

Definition of „Q“, series parallel transformations of lossy circuits, impedance matching using „L“, „PI“ and T networks, Integrated inductors, resistors, Capacitors, tunable inductors, transformers

**MODULE II AMPLIFIER DESIGN 9**

Noise characteristics of MOS devices, Design of CG LNA and inductor degenerated LNAs. Principles of RF Power Amplifiers design.

**MODULE III ACTIVE AND PASSIVE MIXERS 9**

Qualitative Description of the Gilbert Mixer - Conversion Gain, and distortion and noise , analysis of Gilbert Mixer - Switching Mixer - Distortion in Unbalanced Switching Mixer -Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.

**MODULE IV OSCILLATORS 9**

LC Oscillators, Voltage Controlled Oscillators, Ring oscillators, Delay Cells, tuning range in ring oscillators, Tuning in LC oscillators, Tuning sensitivity, Phase Noise in oscillators, sources of phase noise

**MODULE V PLL AND FREQUENCY SYNTHESIZERS 9**

Phase Detector/Charge Pump, Analog Phase Detectors, Digital Phase Detectors, Frequency Dividers, Loop Filter Design, Phase Locked Loops, Phase noise in PLL, Loop Bandwidth, Basic Integer-N frequency synthesizer, Basic Fractional-N frequency synthesizer.

**Total: 45 HOURS**

**REFERENCES**

1. B.Razavi ,“RF Microelectronics” , Prentice-Hall ,1998
2. Bosco H Leung “VLSI for Wireless Communication”, Pearson Education, 2002
3. Behzad Razavi, “Design of Analog CMOS Integrated Circuits” McGraw-Hill, 1999
4. Jia-sheng Hong, "Microstrip filters for RF/Microwave applications", Wiley, 2001
5. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits“, Cambridge University Press ,2003

		<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>P19VL303</b>	<b>Design of Analog Filters and Signal Conditioning Circuits</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

<b>Outcomes</b>				
CO1	Apply the operational and design principles for all the important active analog filter configurations.		K4	M1,M2
CO2	Knowledge of signal conditioning techniques and the necessary guide lines in a Mixed signal IC environment.		K2	M4,M5
CO3	Realize filters based on switched capacitor technique.		K3	M3
CO4	Apply various signal conditioning techniques for interference		K3	M4
CO5	Analyze various signal conditioning Circuits.		K4	M5

**MODULE I FILTER TOPOLOGIES 9**

The Bilinear Transfer Function - Active RC Implementation, Transconductor-C Implementation, Switched Capacitor Implementation, Biquadratic Transfer Function, Active RC implementation, Switched capacitor implementation, High Q, Q peaking and instability, Transconductor-C Implementation, the Digital Biquad.

**MODULE II INTEGRATOR REALIZATION 9**

Lowpass Filters, Active RC Integrators – Effect of finite Op-Amp Gain Bandwidth Product, Active RC SNR, gm-C Integrators, Discrete Time Integrators.

**MODULE III SWITCHED CAPACITOR FILTER REALIZATION 9**

Switched capacitor Technique, Biquadratic SC Filters, SC N-path filters, Finite gain and bandwidth effects, Layout consideration, Noise in SC Filters.

**MODULE IV SIGNAL CONDITIONING TECHNIQUES 9**

Interference types and reduction, Signal circuit grounding, Shield grounding, Signal conditioners for capacitive sensors, Noise and Drift in Resistors, Layout Techniques.

**MODULE V SIGNAL CONDITIONING CIRCUITS 9**

Isolation Amplifiers, Chopper and Low Drift Amplifiers, Electrometer and Transimpedance Amplifiers, Charge Amplifiers, Noise in Amplifiers.

**Total: 45 HOURS**

**REFERENCES**

1. Ramson Pallas-Areny, John G. Webster "Sensors and Signal Conditioning" , A wiley Inter science Publication, John Wiley & Sons INC,2001.
2. R.Jacob Baker, "CMOS Mixed-Signal Circuit Design", John Wiley & Sons, 2008.
3. Schauman, Xiao and Van Valkenburg, "Design of Analog Filters", Oxford University Press, 2009.

		<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>P19VL304</b>	<b>CAD for VLSI Circuits</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

<b>Outcomes</b>			
CO1	Understand the VLSI design methodologies and the concept behind the combinatorial optimization	K2	M1
CO2	Understanding the various types of graph model, layouts and data structure algorithms	K2	M2
CO3	Develop problem solving skills for partitioning and routing algorithms	K3	M3
CO4	Understand and simulate the modeling levels	K2	M4
CO5	Develop problem solving skills in synthesis process	K3	M5

**MODULE I INTRODUCTION TO VLSI DESIGN FLOW 9**

Introduction to VLSI Design methodologies, Basics of VLSI design automation tools, Algorithmic Graph Theory and Computational Complexity, Tractable and Intractable problems, General purpose methods for combinatorial optimization.

**MODULE II LAYOUT, PLACEMENT AND PARTITIONING 9**

Layout Compaction, Design rules, Problem formulation, Algorithms for constraint graph compaction, Placement and partitioning, Circuit representation, Placement algorithms, Partitioning

**MODULE III FLOOR PLANNING AND ROUTING 9**

Floor planning concepts, Shape functions and floorplan sizing, Types of local routing problems, Area routing, Channel routing, Global routing, Algorithms for global routing.

**MODULE IV SIMULATION AND LOGIC SYNTHESIS 9**

Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis.

**MODULE V HIGH LEVEL SYNTHESIS 9**

Hardware models for high level synthesis, internal representation, allocation, assignment and scheduling, scheduling algorithms, Assignment problem, High level transformations.

**Total: 45 HOURS**

**REFERENCES**

1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.
2. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.
3. Sadiq M. Sait, Habib Youssef, "VLSI Physical Design automation: Theory and Practice", World Scientific 1999.
4. Steven M. Rubin, "Computer Aids for VLSI Design", Addison Wesley Publishing 1987.

**SEMESTER I – ELECTIVE II**

		<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>P19VL305</b>	<b>Embedded System Design</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

<b>Outcomes</b>			
CO1	Understand the architecture and design involved in design of embedded systems	K2	M1
CO2	Program ARM processor	K3	M2
CO3	Understand the embedded system network architecture	K2	M3
CO4	Analyze the problems in real time implementation of embedded systems and its solutions	K4	M4
CO5	Understand the concepts of system design technologies	K2	M5

**MODULE I EMBEDDED SYSTEM OVERVIEW 9**

Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Single-Purpose Processors.

**MODULE II GENERAL AND SINGLE PURPOSE PROCESSOR 9**

Basic Architecture, Pipelining, Superscalar and VLIW architectures, Programmer's view, Development Environment, Application-Specific Instruction-Set Processors (ASIPs) Microcontrollers, Timers, Counters and watchdog Timer, UART, LCD Controllers and Analog-to-Digital Converters, Memory Concepts.

**MODULE III BUS STRUCTURES 9**

Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus-Based I/O, Arbitration, Serial Protocols, I2C, CAN and USB, Parallel Protocols – PCI and ARM Bus, Wireless Protocols – IrDA, Bluetooth, IEEE 802.11.

**MODULE IV STATE MACHINE AND CONCURRENT PROCESS MODELS 9**

Basic State Machine Model, Finite-State Machine with Datapath Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, Dataflow Model, Real-time Systems, Automation: Synthesis, Verification : Hardware/Software Co-Simulation, Reuse: Intellectual Property Cores, Design Process Models.

**MODULE V EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS 9**

Compilation Process – Libraries – Porting kernels – C extensions for embedded systems – emulation and debugging techniques – RTOS – System design using RTOS.

**Total: 45 HOURS**

**REFERENCES**

1. Bruce Powel Douglas, "Real time UML, second edition: Developing efficient objects for embedded systems", 3rd Edition 1999, Pearson Education.
2. Daniel W. Lewis, "Fundamentals of embedded software where C and assembly meet", Pearson Education, 2002.
3. Frank Vahid and Tony Gwargie, "Embedded System Design", John Wiley & sons, 2002.
4. Steve Heath, "Embedded System Design", Elsevier, Second Edition, 2004.

		<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>P19VL306</b>	<b>Advanced Microprocessors and Architectures</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

<b>Outcomes</b>			
CO1	Understand the fundamentals and architecture of microprocessor	K2	M1
CO2	Understand the CISC architecture-Pentium	K2	M2
CO3	Understand ARM architecture and processors	K2	M3
CO4	Describe the fundamentals of Motorola microcontrollers	K3	M4
CO5	Know the CPU architecture and details of PIC microcontroller	K2	M5

**MODULE I 80386 AND PENTIUM PROCESSOR 9**

80386 PROCESSOR: Basic programming model – Memory organization – Data types – Instruction set – Addressing mode – Address translation – Interrupts –PENTIUM PROCESSOR : Introduction to Pentium processor architecture – Special Pentium Registers – Pentium Memory Management – Introduction to Pentium pro processor – Pentium Pro Special Features.

**MODULE II CISC and RISC Architecture 9**

Introduction to RISC architectures: RISC Versus CISC – RISC Case studies: MIPS R4000 – SPARC – Intel i860 – IBM RS/6000.

**MODULE III ARM PROCESSOR 9**

ARM Programmer’s Model – Registers – Processor Modes – State of the processor – Condition Flags – ARM Pipelines – Exception Vector Table – ARM Processor Families – Typical 3 stage pipelined ARM organization– Introduction to ARM Memory Management Unit.

**MODULE IV ARM ADDRESSING MODES AND INSTRUCTION SET 9**

ARM Addressing Modes – ARM Instruction Set Overview – Thumb Instruction Set Overview – LPC210X ARM Processor Features.

**MODULE V PIC MICROCONTROLLER AND MOTOROLA 68HC11 MICROCONTROLLER 9**

Instruction set, addressing modes – operating modes- Interrupt system- RTC-Serial Communication Interface – A/D Converter PWM and UART. MOTOROLA: CPU Architecture – Instruction set – interrupts- Timers- I 2C Interfacing –UART- A/D Converter – PWM

**Total: 45 HOURS**

**REFERENCES**

1. Andrew Sloss, "ARM System Developer's Guide", Morgan Kaufmann Publishers, 2005
2. Barry B Brey, "The Intel Microprocessor, Pentium and Pentium Pro Processor, Architecture Programming and Interfacing", Prentice Hall of India, 2002.
3. Daniel Tabak, "Advanced Microprocessors", McGraw Hill Inc., 1995.
4. David E Simon "An Embedded Software Primer", Pearson Education, 2007
5. Gene .H.Miller ." Micro Computer Engineering ," Pearson Education , 2003.
6. Intel, "Microprocessors, Vol-I & Vol-II", Intel Corporation, USA, 1992.
7. John .B.Peatman , " Design with PIC Microcontroller , Prentice hall, 1997
8. Mohammed Rafiquzzaman, "Microprocessors and Microcomputer Based System Design", Universal Book Stall, New Delhi, 1990.
9. Steve Furber, "ARM System-on-Chip Architecture", Pearson Education, 2005 "ARM7 TDMI Technical Reference Manual", ARM Ltd., UK, 2004 6.

		<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>P19VL307</b>	<b>DSP Processor Architecture and Programming</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

<b>Outcomes</b>			
CO1	Describe the fundamentals of Digital Signal Processors.	K2	M1
CO2	Explain the architecture, addressing modes and instruction set of generic DSP devices.	K4	M2
CO3	Illustrate algorithms for implementation in Digital Signal Processors to solve real-time problems.	K4	M3
CO4	Compare the features and performance of DSP devices.	K4	M4
CO5	Identify salient features of advanced DSP devices.	K3	M5

**MODULE I FUNDAMENTALS OF PROGRAMMABLE DSPs 9**

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in PDSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

**MODULE II TMS320C5X PROCESSOR 9**

Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals.

**MODULE III TMS320C6X PROCESSOR 9**

Architecture of the C6x Processor - Instruction Set - DSP Development System: Introduction – DSP Starter Kit Support Tools- Code Composer Studio - Support Files - Programming Examples to Test the DSK Tools – Application Programs for processing real time signals.

**MODULE IV ADSP PROCESSORS 9**

Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.

**MODULE V ADVANCED PROCESSORS 9**

Architecture of TMS320C54X: Pipe line operation, Code Composer studio – Architecture of TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.

**Total: 45 HOURS**

**REFERENCES**

1. Avtar Singh and S. Srinivasan, Digital Signal Processing – Implementations using DSP Microprocessors with Examples from TMS320C54xx, cengage Learning India Private Limited, Delhi 2012
2. B.Venkataramani and M.Bhaskar, "Digital Signal Processors – Architecture, Programming and Applications" – Tata McGraw – Hill Publishing Company Limited. New Delhi, 2003.
3. RulphChassaing, Digital Signal Processing and Applications with the C6713 and C6416 DSK, A John Wiley & Sons, Inc., Publication, 2005
4. User guides Texas Instrumentation, Analog Devices, Motorola.



		<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>P19VL308</b>	<b>Digital Control Engineering</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

<b>Outcomes</b>			
CO1	Describe continuous time and discrete time controllers analytically.	K2	M1,M2
CO2	Define and state basic analog to digital and digital to analog conversion principles	K2	M2
CO3	Analyze sampled data control system in time and frequency domains.	K4	M3
CO4	Design simple PI, PD, PID continuous and digital controllers.	K6	M1,M4
CO5	Develop schemes for practical implementation of temperature and motor control systems.	K3	M5

**MODULE I CONTROLLERS IN FEEDBACK SYSTEMS 9**

Review of frequency and time response analysis and specifications of first order and second order feedback control systems, need for controllers, continuous time compensations, continuous time PI, PD, PID controllers, digital PID controllers.

**MODULE II BASIC DIGITAL SIGNAL PROCESSING IN CONTROL SYSTEMS 9**

Sampling theorem, quantization, aliasing and quantization error, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction.

**MODULE III MODELING OF SAMPLED DATA CONTROL SYSTEM 9**

Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury's stability test, state space description, first companion, second companion, Jordan canonical models, discrete state variable models (elementary principles only).

**MODULE IV DESIGN OF DIGITAL CONTROL ALGORITHMS 9**

Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

**MODULE V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS 9**

Algorithm development of PID control algorithms, standard programmes for microcontroller implementation, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems, DSP implementation of motor control system.

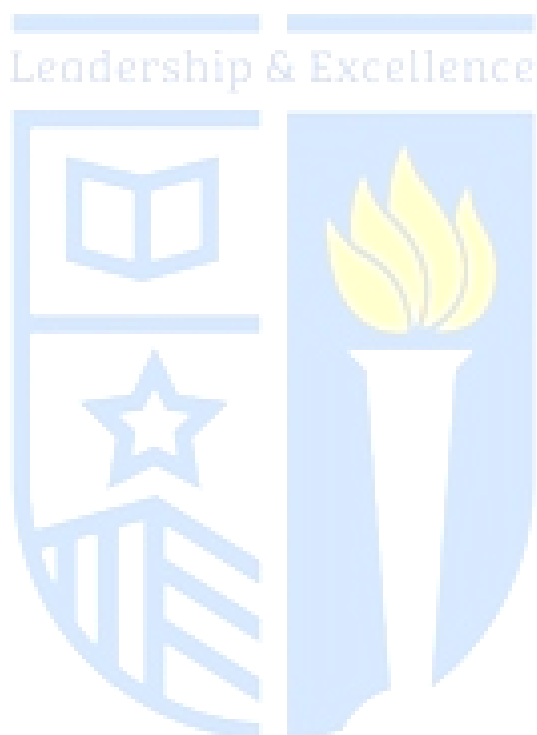
**Total: 45 HOURS**

**REFERENCES**

1. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill,1995.
2. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996.
3. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997.

**Semester II**

Sl.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
<b>THEORY</b>								
1	P19VL104	Analog IC Design	PC	4	4	0	0	4
2	P19VL105	Low Power VLSI Design	PC	3	3	0	0	3
3	P19VL106	Testing of VLSI Circuits	PC	3	3	0	0	3
4	P19VL3XX	Program Elective III	PE	3	3	0	0	3
5	P19VL3XX	Program Elective IV	PE	3	3	0	0	3
<b>PRACTICALS</b>								
6	P19VL112	VLSI Design Laboratory II	PC	4	0	0	4	2
7	P19VL201	Mini Project	PW	4	0	0	4	2
8	P19AC5XX	Audit Course II	AC	2	2	0	0	NC
<b>TOTAL</b>				<b>26</b>	<b>18</b>	<b>0</b>	<b>8</b>	<b>20</b>



		<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>19VL104</b>	<b>ANALOG IC DESIGN</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

<b>Outcomes</b>			
CO1	<b>(Analyze)</b> Analyze single stage amplifiers with MOS loads.	K4	M1
CO2	<b>(Analyze)</b> Analyze the concepts of frequency response and noise characteristics of differential amplifiers.	K4	M2
CO3	<b>(Create)</b> Design and model different active devices with OPAMPs.	K6	M3
CO4	<b>(Understand)</b> Interpret the multi-pole systems, frequency compensations techniques.	K2	M4
CO5	<b>(Create)</b> Design analog circuits using CMOS technology.	K6	M5

#### **MODULE-I MOSFET METRICS**

**9**

Simple long channel MOSFET theory – SPICE Models – Technology trend, Need for Analog design - Sub-micron transistor theory, Short channel effects, Narrow width effect, Drain induced barrier lowering, Sub-threshold conduction, Reliability, Digital metrics, Analog metrics, Small signal parameters, Unity Gain Frequency, Miller's approximation

#### **MODULE-II SINGLE STAGE AND TWO STAGE AMPLIFIERS**

**9**

Single Stage Amplifiers – Common source amplifier with resistive load, diode load, constant current load, Source degeneration Source follower, Input and output impedance, Common gate amplifier - Differential Amplifiers – differential and common mode response, Input swing, gain, diode load and constant current load - Basic Two Stage Amplifier, Cut-off frequency, poles and zeros

#### **MODULE III FREQUENCY RESPONSE OF SINGLE STAGE AND TWO STAGE AMPLIFIERS**

**9**

Frequency Response of Single Stage Amplifiers – Noise in Single stage Amplifiers – Stability and Frequency Compensation in Single stage Amplifiers, Frequency Response of Two Stage Amplifiers, – Noise in two stage Amplifiers – Stability, gain and phase margins, Frequency Compensation in two stage Amplifiers, Effect of loading in feedback networks

#### **MODULE-IV CURRENT MIRRORS AND REFERENCE CIRCUITS**

**9**

Cascode, Negative feedback, Wilson, Regulated cascode, Bandgap voltage reference, Constant Gm biasing, supply and temperature independent reference, curvature compensation, trimming, Effect of transistor mismatch in analog design

#### **MODULE -V OP AMPS**

**9**

Gilbert cell and applications, Basic two stage OPAMP, two-pole system response, common mode and differential gain, Frequency response of OPAMP, CMFB circuits, slew rate, power supply rejection ratio, random offset, systematic offset, Noise, Output stage, OTA and OPAMP circuits - Low voltage OPAMP

**Total: 45 HOURS**

#### **REFERENCES:**

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2000
2. Philip E.Allen, "CMOS Analog Circuit Design", Oxford University Press, 2013
3. Paul R.Gray, "Analysis and Design of Analog Integrated Circuits", Wiley Student edition, 5th edition, 2009.
4. R.Jacob Baker, "CMOS: Circuit Design, Layout , and Simulation", Wiley Student Edition, 2009
5. Willey M.C. Sansen, "Analog design essentials", Springer, 2006.
6. Grebene, "Bipolar and MOS Analog Integrated circuit design", John Wiley & Sons Inc., 2003.

		<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>P19VL105</b>	<b>LOW POWER VLSI DESIGN</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

<b>Outcomes</b>				
CO1	<b>(Apply)</b> Identify the sources of power dissipation in digital IC systems. Understand the impact of power on system performance and reliability		K3	M1
CO2	<b>(Analyze)</b> Examine various power optimization algorithms in low power VLSI design system		K4	M2
CO3	<b>(Create)</b> Design of low power CMOS circuits		K6	M3
CO4	<b>(Apply)</b> Apply probabilistic analysis to characterize dynamic power estimation		K3	M4
CO5	<b>(Create)</b> Design low power VLSI circuits and apply the techniques in different applications.		K6	M5

**MODULE-I POWER DISSIPATION IN CMOS 9**

Physics of power dissipation in CMOS FET devices – Hierarchy of limits of power – Sources of power consumption – Static Power Dissipation, Active Power Dissipation - Designing for Low Power, Circuit Techniques For Leakage Power Reduction - Basic principle of low power design.

**MODULE-II POWER OPTIMIZATION 9**

Logic level power optimization – Circuit level low power design – Standard Adder Cells, CMOS Adders Architectures-BiCMOS adders - Low Voltage Low Power Design Techniques, Current Mode Adders -Types Of Multiplier Architectures, Braun, Booth and Wallace Tree Multipliers and their performance comparison

**MODULE III DESIGN OF LOW POWER CMOS CIRCUITS 9**

Computer arithmetic techniques for low power system – low voltage low power static Random access and dynamic Random access memories – low power clock, Inter connect and layout design – Advanced techniques – Special techniques.

**MODULE IV POWER ESTIMATION 9**

Power Estimation techniques – logic power estimation – Simulation power analysis – Probabilistic power analysis.

**MODULE V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER 9**

Synthesis for low power – Behavioral level transform – software design for low power.

**Total: 45 HOURS**

**REFERENCES:**

1. P. Rashinkar, Paterson and L. Singh, "Low Power Design Methodologies", Kluwer Academic, 2002
2. Kaushik Roy, Sharat Prasad, "Low power CMOS VLSI circuit design", John Wiley sons Inc., 2000.
3. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley, 1999.
4. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer, 1995
5. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.
6. AbdelatifBelaouar, Mohamed.I.Elmasry, "Low power digital VLSI design", Kluwer, 1995.
7. DimitriosSoudris, C.Pignet, Costas Goutis, "Designing CMOS Circuits for Low Power" Kluwer, 2002.
8. Kiat-send Yeo, Kaushik Roy "Low-Voltage, Low-power VLSI Subsystem", Tata McGraw-Hill, 2009

		<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>P19VL106</b>	<b>TESTING OF VLSI CIRCUITS</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

<b>Outcomes</b>			
CO1	<b>(Understand)</b> Interpret the importance of testing and its types in VLSI circuits	K2	M1
CO2	<b>(Analyze)</b> Analyze the testing of sequential and combinational circuits	K4	M2
CO3	<b>(Apply)</b> Model different faults and carry out fault simulation in digital circuits	K3	M3
CO4	<b>(Apply)</b> Ability to determine fault oriented test vectors for single stuck-at-faults in combinational and Sequential circuits.	K3	M3,M5
CO5	<b>(Create)</b> Ability to design digital VLSI circuits with DFT and BIST techniques	K6	M4

**MODULE I TESTING AND FAULT MODELLING 9**

Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation – Delay models – Gate Level Event – driven simulation.

**MODULE II TEST GENERATION 9**

Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.

**MODULE III DESIGN FOR TESTABILITY 9**

Design for Testability – Ad-hoc design – generic scan based design – classical scan based design– system level DFT approaches.

**MODULE IV SELF – TEST AND TEST ALGORITHMS 9**

Built-In self-test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.

**MODULE V FAULT DIAGNOSIS 9**

Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits– Self-checking design – System Level Diagnosis.

**Total: 45 HOURS**

**REFERENCES**

1. A.L.Crouch, "Design Test for Digital IC's and Embedded Core Systems", Prentice Hall International, 2002.
2. M.Abramovici, M.A.Breuer and A.D. Friedman, "Digital systems and Testable Design", Jaico Publishing House, 2002.
3. M.L.Bushnell and V.D.Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed- Signal VLSI Circuits", Kluwer Academic Publishers, 2002.
4. P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.

<b>P19VL112</b>	<b>VLSI Design Laboratory -II</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		<b>0</b>	<b>0</b>	<b>4</b>	<b>2</b>

<b>Outcomes</b>	Upon completion of this course, students will be able to			
	CO1	The student would have hands on experience in the carrying out a complete VLSI based experiments using / CADENCE/ TANNER/ Mentor/Synopsis		K3

#### List of Experiments

1. To synthesize and understand the Boolean optimization in synthesis.
2. Static timing analyses procedures and constraints.
3. Critical path considerations. Scan chain insertion, Floor planning, Routing and Placement procedures.
4. Power planning, Layout generation, LVS and back annotation, Total power estimate.
5. Analog circuit simulation. Simulation of logic gates, Current mirrors, Current sources, Differential amplifier in Spice.
6. Layout generations, LVS, Back annotation

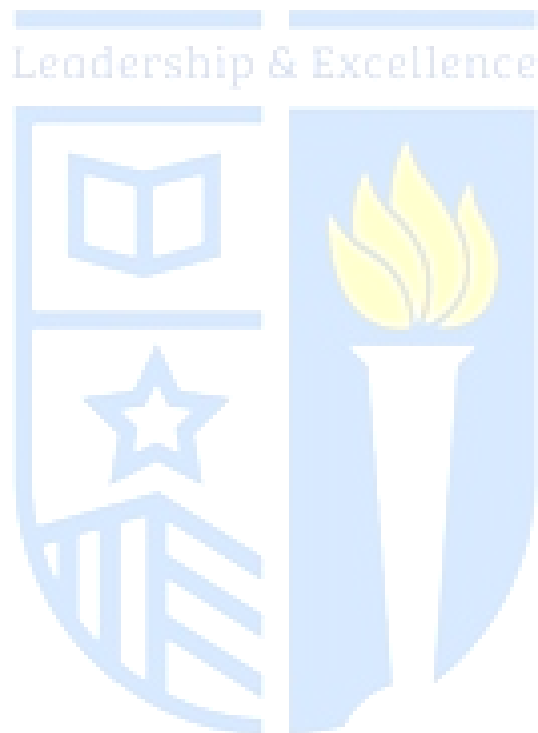
**Total: 45 HOURS**

#### REFERENCES

1. Ming-Bo Lin, Digital System Designs and Practices using Verilog HDL and FPGAs, Wiley, 2012.
2. Samir Palnitkar, Verilog HDL, Pearson Education, 2ndEdition, 2004.
3. J.Bhaskar, A VHDL Primer, Prentice Hall, 1998.
4. M.H.Rashid, Spice for Circuits and Electronics using Pspice, PHI 1995.
5. M.J.S.Smith, Application Specific Integrated Circuits, Pearson Education, 2008.

**PROGRAM ELECTIVES (PE)**

Sl.No	Course Code	Course Title	Course Category	L	T	P	C
<b>SEMESTER II – ELECTIVE III</b>							
1	P19VL309	DSP Integrated Circuits	PE	3	0	0	3
2	P19VL310	VLSI Signal Processing	PE	3	0	0	3
3	P19VL311	Soft Computing and Optimization Techniques	PE	3	0	0	3
4	P19VL312	Reconfigurable Architectures	PE	3	0	0	3
<b>SEMESTER II – ELECTIVE IV</b>							
1	P19VL313	CMOS Digital VLSI Design	PE	3	0	0	3
2	P19VL314	Networks on Chip	PE	3	0	0	3
3	P19VL315	Design and Analysis of Computer Algorithms	PE	3	0	0	3
4	P19VL316	Digital Image Processing	PE	3	0	0	3



**SEMESTER II - ELECTIVE III**

<b>P19VL309</b>	<b>DSP INTEGRATED CIRCUITS</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

<b>Outcomes</b>				
CO1	Get to know about the Digital Signal Processing concepts and its algorithms		K2	M1
CO2	Get an idea about finite word length effects in digital filters		K2	M2
CO3	Concept behind multi rate systems is understood.		K4	M2
CO4	Get familiar with the DSP processor architectures and how to perform synthesis of processing elements		K4	M3,M4
CO5	Implementation of digital signal processing and Number systems		K5	M5

**MODULE I INTRODUCTION TO DSP INTEGRATED CIRCUITS 9**

Introduction to Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal-processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT Algorithm, Image coding, Discrete cosine transforms, Standard digital signal processors, Application specific ICs for DSP, DSP systems, DSP system design, Integrated circuit design.

**MODULE II DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9**

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multi rate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multi rate filters. Finite word length effects - Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

**MODULE III DSP ARCHITECTURES 9**

DSP system architectures, Standard DSP architecture-Harvard and Modified Harvard architecture. Ideal DSP architectures, Multiprocessors and multi computers, Systolic and Wave front arrays, Shared memory architectures.

**MODULE IV SYNTHESIS OF DSP ARCHITECTURES 9**

Synthesis: Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs. Combinational & sequential networks- Storage elements – clocking of synchronous systems, Asynchronous systems -FSM

**MODULE V ARITHMETIC UNIT AND PROCESSING ELEMENTS 9**

Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Digit Serial arithmetic, CORDIC Algorithm, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Case Study: DCT and FFT processor

**Total: 45 HOURS**

**REFERENCES**

1. B.Venkatramani, M.Bhaskar, "Digital Signal Processors", Tata McGraw-Hill, 2002
2. John J. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", Pearson Education, 2002
3. Keshab Parhi, "VLSI Digital Signal Processing Systems design & Implementation", John Wiley & Sons, 1999.
4. Lars Wanhammer, "DSP Integrated Circuits", Academic press, New York, 1999.



P19VL310	VLSI Signal Processing	L	T	P	C
		3	0	0	3

Upon completion of this course, students will be able to

Outcomes			
CO1	Represent DSP algorithms, define and compute iteration bound of an algorithm.	K2	M1
CO2	Use Pipelining and parallel processing methodologies in FIR filters	K3	M1
CO3	Apply retiming, unfolding techniques.	K3	M2,M3
CO4	Design systolic architecture.	K5	M4
CO5	Apply strength reduction in filters and transforms.	K3	M5

**MODULE I PIPELINING AND PARALLEL PROCESSING OF DIGITAL FILTERS 9**

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs – critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

**MODULE II ALGORITHMIC STRENGTH REDUCTION TECHNIQUE I 9**

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters

**MODULE III ALGORITHMIC STRENGTH REDUCTION -II 9**

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with powerof-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

**MODULE IV BIT-LEVEL ARITHMETIC ARCHITECTURES 9**

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon’s bit-serial multipliers using Horner’s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner’s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

**MODULE V NUMERICAL STRENGTH REDUCTION, WAVE AND ASYNCHRONOUS PIPELINING 9**

Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

**Total: 45 HOURS**

**REFERENCES**

1. Keshab K. Parhi, " VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.
2. U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004.

<b>P19VL311</b>	<b>Soft Computing and Optimization Techniques</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>
Upon completion of this course, students will be able to					
<b>Outcomes</b>	CO1	Implement machine learning through Neural networks.		K3	M1
	CO2	Develop a Fuzzy expert system.		K5	M2
	CO3	Model Neuro Fuzzy system for clustering and classification.		K5	M3
	CO4	Use the optimization techniques to solve the real world problems		K3	M4
	CO5	Analyze the Genetic algorithm and its optimization		K4	M5
<b>MODULE I</b>	<b>NEURAL NETWORKS</b>	<b>9</b>			
Machine Learning using Neural Network, Learning algorithms, Supervised Learning Neural Networks – Feed Forward Networks, Radial Basis Function, Unsupervised Learning Neural Networks – Self Organizing map , Adaptive Resonance Architectures, Hopfield network					
<b>MODULE II</b>	<b>FUZZY LOGIC</b>	<b>9</b>			
Fuzzy Sets – Operations on Fuzzy Sets – Fuzzy Relations – Membership Functions-Fuzzy Rules and Fuzzy Reasoning – Fuzzy Inference Systems – Fuzzy Expert Systems – Fuzzy Decision Making					
<b>MODULE III</b>	<b>NEURO-FUZZY MODELING</b>	<b>9</b>			
Adaptive Neuro-Fuzzy Inference Systems – Coactive Neuro-Fuzzy Modeling – Classification and Regression Trees – Data Clustering Algorithms – Rule base Structure Identification –Neuro-Fuzzy Control – Case Studies.					
<b>MODULE IV</b>	<b>CONVENTIONAL OPTIMIZATION TECHNIQUES</b>	<b>9</b>			
Introduction to optimization techniques, Statement of an optimization problem, classification, Unconstrained optimization-gradient search method-Gradient of a function, steepest gradient-conjugate gradient, Newton’s Method, Marquardt Method, Constrained optimization –sequential linear programming, Interior penalty function method, external penalty function method.					
<b>MODULE V</b>	<b>EVOLUTIONARY OPTIMIZATION TECHNIQUES</b>	<b>9</b>			
Genetic algorithm - working principle, Basic operators and Terminologies, Building block hypothesis, Travelling Salesman Problem, Particle swam optimization, Ant colony optimization.					
<b>Total:</b>			<b>45 HOURS</b>		

**REFERENCES**

1. David E. Goldberg, Genetic Algorithms in Search, Optimization and Machine Learning, Addison wesley, 2009.
2. George J. Klir and Bo Yuan, Fuzzy Sets and Fuzzy Logic-Theory and Applications,Prentice Hall, 1995.
3. James A. Freeman and David M. Skapura, Neural Networks Algorithms, Applications, and Programming Techniques, Pearson Edn., 2003.
4. Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, Neuro-Fuzzy and Soft Computing, PrenticeHall of India, 2003.
5. Mitchell Melanie, An Introduction to Genetic Algorithm, Prentice Hall, 1998
6. Simon Haykins, Neural Networks: A Comprehensive Foundation, Prentice Hall International Inc, 1999.
7. Singiresu S. Rao, Engineering optimization Theory and practice, John Wiley & sons, inc,Fourth Edition, 2009
8. Timothy J.Ross, Fuzzy Logic with Engineering Applications, McGraw-Hill, 1997.
9. Venkata Rao, Vimal J. Savsani, Mechanical Design Optimization Using Advanced Optimization Techniques, springer 2012.

<b>P19VL312</b>	<b>Reconfigurable Architectures</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>
	Upon completion of this course, students will be able to				
<b>Outcomes</b>	CO1 Compare FPGA routing architectures			K4	M1
	CO2 Discuss FPGA applications			K2	M2,M5
	CO3 Explain high level synthesis			K3	M4
	CO4 Determine the Programmable logic cells.			K3	M3,M5
	CO5 Design SoC using VHDL and Verilog HDL coding.			K6	M4,M5
<b>MODULE I</b>	<b>INTRODUCTION</b>				<b>9</b>
Domain-specific processors, Application specific processors, Reconfigurable Computing Systems – Evolution of reconfigurable systems – Characteristics of RCS advantages and issues. Fundamental concepts & Design steps –classification of reconfigurable architecture-fine, coarse grain & hybrid architectures – Examples					
<b>MODULE II</b>	<b>FPGA TECHNOLOGIES &amp; ARCHITECTURE</b>				<b>9</b>
Technology trends- Programming technology- SRAM programmed FPGAs, antifuse programmed FPGAs, erasable programmable logic devices. Alternative FPGA architectures: Mux Vs LUT based logic blocks – CLB Vs LAB Vs Slices- Fast carry chains- Embedded RAMs- FPGA Vs ASIC design styles.					
<b>MODULE III</b>	<b>ROUTING FOR FPGAS</b>				<b>9</b>
General Strategy for routing in FPGAs- routing for row-based FPGAs – segmented channel routing, definitions- Algorithm for I segment and K segment routing – Routing for symmetrical FPGAs, Flexibility of FPGA Routing Architectures: FPGA architectural flexibility on Routability- Effect of switch block flexibility on routability - Tradeoffs in flexibility of S and C blocks					
<b>MODULE IV</b>	<b>HIGH LEVEL DESIGN</b>				<b>9</b>
FPGA Design style: Technology independent optimization- technology mapping- Placement. Highlevel synthesis of reconfigurable hardware, high- level languages, Design tools: Simulation (cycle based, event driven based) – Synthesis (logic/HDL vs physically aware) – timing analysis (static vs dynamic)- verification physical design tools.					
<b>MODULE V</b>	<b>APPLICATION DEVELOPMENT WITH FPGAS</b>				<b>9</b>
Case Studies of FPGA Applications–System on a Programmable Chip (SoPC) Designs.					
<b>Total:</b>				<b>45 HOURS</b>	

**REFERENCES**

1. Christophe Bobda, "Introduction to Reconfigurable Computing –Architectures, Algorithms and Applications", Springer, 2010.
2. Clive "Max" Maxfield, "The Design Warrior's Guide to FPGAs: Devices, Tools And Flows", Newnes, Elsevier, 2006.
3. Jorgen Staunstrup, Wayne Wlf, "Hardware/Software Co- Design: Priciples and practice", Kluwer Academic Pub, 1997.
4. Maya B. Gokhale and Paul S. Graham, "Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays", Springer, 2005.
5. Russell tessier and Wayne Burlson "Reconfigurable Computing for Digital Signal Processing: A Survey" Journal of VLSI Signal processing 28,p7-27,2001.
6. Stephen M. Trimmerger, "field – programmable Gate Array Technology" Springer,2007.
7. Stephen D. broen, Robert J. Francis, Jonathan Rose, Zvonko G. Vranesic," Fieldprogrammable Gate Arrays", Kluwer Academic Publishers, 1992.
8. Scott Hauck and Andre Dehon (Eds.), "Reconfigurable Computing –The Theory and Practice of FPGA- Based Computation", Elsevier / Morgan Kaufmann, 2008.

**SEMESTER II - ELECTIVE IV**

		<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>P19VL313</b>	<b>CMOS DIGITAL VLSI DESIGN</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

<b>Outcomes</b>			
CO1	Carry out transistor level design of the most important building blocks used in digital CMOS VLSI circuits.	K3	M1
CO2	Design static and dynamic circuits with the aid of design rules.	K6	M2
CO3	Design latches and registers by analyzing timing issues.	K6	M3
CO4	Discuss design methodology of arithmetic building block	K4	M4
CO5	Analyze tradeoffs of the various circuit choices for each of the building block.	K4	M5

**MODULE I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 9**

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, Technology Scaling - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters.

**MODULE II COMBINATIONAL LOGIC CIRCUITS 9**

Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

**MODULE III SEQUENTIAL LOGIC CIRCUITS 9**

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pulse and sense amplifier based Registers, Non bistable Sequential Circuits.

**MODULE IV ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES 9**

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

**MODULE V INTERCONNECT AND CLOCKING STRATEGIES 9**

Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design.

**Total: 45 HOURS**

**REFERENCES:**

1. Jan Rabaey, Anantha Chandrakasan, B Nikolic, "Digital Integrated Circuits: A Design Perspective". Second Edition, Feb 2003, Prentice Hall of India.
2. Jacob Baker "CMOS: Circuit Design, Layout, and Simulation, Third Edition", Wiley IEEE Press 2010 3rd Edition.
3. M J Smith, "Application Specific Integrated Circuits", Addison Wesley, 1997
4. N.Weste, K. Eshraghian, " Principles of CMOS VLSI Design". Second Edition, 1993 Addison Wesley.

		<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>P19VL314</b>	<b>Networks on Chip</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

<b>Outcomes</b>			
CO1	Compare different architecture design	K4	M1,M2
CO2	Discuss different routing algorithms	K2	M3
CO3	Explain three dimensional networks - on-chip architectures	K4	M5
CO4	Analyze test and fault tolerance of Communications in NOC	K4	M4
CO5	Apply the 3D Integration procedures in NOC	K3	M5

**MODULE I INTRODUCTION TO NOC 9**

Introduction to NoC – OSI layer rules in NoC - Interconnection Networks in Network-on-Chip Network Topologies - Switching Techniques - Routing Strategies - Flow Control Protocol Quality-of-Service Support

**MODULE II ARCHITECTURE DESIGN 9**

Switching Techniques and Packet Format - Asynchronous FIFO Design -GALS Style of Communication - Wormhole Router Architecture Design - VC Router Architecture Design - Adaptive Router Architecture Design.

**MODULE III ROUTING ALGORITHM 9**

Packet routing-Qos, congestion control and flow control – router design – network link design – Efficient and Deadlock-Free Tree-Based Multicast Routing Methods - Path-Based Multicast Routing for 2D and 3D Mesh Networks- Fault-Tolerant Routing Algorithms - Reliable and Adaptive Routing Algorithms

**MODULE IV TEST AND FAULT TOLERANCE OF NOC 9**

Design-Security in Networks-on-Chips-Formal Verification of Communications in Networks-on Chips Test and Fault Tolerance for Networks-on-Chip Infrastructures-Monitoring Services for Networks-on Chips.

**MODULE V THREE-DIMENSIONAL INTEGRATION OF NETWORK-ON-CHIP 9**

Three-Dimensional Networks-on-Chips Architectures. – A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures - Resource Allocation for QoS On-Chip Communication – Networks-on-Chip Protocols-On-Chip Processor Traffic Modeling for Networks-on Chip

**Total: 45 HOURS**

**REFERENCES:**

1. ChrysostomosNicolopoulos, Vijaykrishnan Narayanan, Chita R.Das" Networks-on - Chip " Architectures Holistic Design Exploration", Springer.
2. Fayezgebali, Haythamelmiligi, HqhahedWatheq E1-Kharashi "Networks-on-Chips theory and practice CRC press.
3. Konstantinos Tatas and Kostas Siozios "Designing 2D and 3D Network-on-Chip Architectures" 2013
4. Palesi, Maurizio, Daneshtalab, Masoud "Routing Algorithms in Networks-on-Chip" 2014
5. SantanuKundu, SantanuChattopadhyay "Network-on-Chip: The Next Generation of System on-Chip Integration",2014 CRC Press

<b>P19VL315</b>	<b>DESIGN AND ANALYSIS OF COMPUTER ALGORITHMS</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

<b>Outcomes</b>			
CO1	Apply the suitable algorithm according to the given optimization problem.	K3	M1
CO2	Ability to modify the algorithms to refine the complexity parameters.	K4	M2
CO3	Understand the various algorithms for searching and sorting.	K2	M3
CO4	Apply the graph algorithms in path of circuits.	K3	M4
CO5	Understanding of parallel algorithms and Genetic algorithms.	K2	M5

**MODULE I INTRODUCTION 9**

Polynomial and Exponential algorithms, big "oh" and small "oh" notation, exact algorithms and heuristics, direct / indirect / deterministic algorithms, static and dynamic complexity, stepwise refinement.

**MODULE II DESIGN TECHNIQUES 9**

Subgoals method, working backwards, work tracking, branch and bound algorithms for traveling salesman problem and knapsack problem, hill climbing techniques, divide and conquer method, dynamic programming, greedy methods.

**MODULE III SEARCHING AND SORTING 9**

Sequential search, binary search, block search, Fibonacci search, bubble sort, bucket sorting, quick sort, heap sort, average case and worst case behavior

**MODULE IV GRAPH ALGORITHMS 9**

Minimum spanning, tree, shortest path algorithms, R-connected graphs, Even's and Kleitman's algorithms, max-flow min cut theorem, Steiglitz's link deficit algorithm.

**MODULE V SELECTED TOPICS 9**

NP Completeness Approximation Algorithms, NP Hard Problems, Strassen's Matrix Multiplication Algorithms, Magic Squares, Introduction To Parallel Algorithms and Genetic Algorithms, Monte-Carlo Methods, Amortised Analysis.

**Total: 45 HOURS**

**REFERENCES:**

1. D.E.Goldberg, "Genetic Algorithms : Search Optimization and Machine Learning", Addison Wesley, 1989.
2. E.Horowitz and S.Sahni, "Fundamentals of Computer Algorithms", Galgotia Publications, 1988.
3. Sara Baase, "Computer Algorithms : Introduction to Design and Analysis", Addison Wesley, 1988.
4. T.H.Cormen, C.E.Leiserson and R.L.Rivest, "Introduction to Algorithms", Mc Graw Hill, 1994.

		<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>P19VL316</b>	<b>Digital Image Processing</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>
<b>Outcomes</b>	Upon completion of this course, students will be able to				
	CO1 Employ color image processing techniques.			K3	M4
	CO2 Apply morphological image processing algorithms.			K3	M2
	CO3 Apply segmentation algorithms and descriptors for image processing.			K3	M3
	CO4 Demonstrate knowledge of image acquisition and digitization for enhancement			K2	M1
CO5 Apply compression, watermarking and steganography algorithms to images.			K4	M5	

**MODULE I DIGITAL IMAGE FUNDAMENTALS 9**

A simple image model, Sampling and Quantization, Imaging Geometry, Digital Geometry, Image Acquisition Systems, Different types of digital images. Basic concepts of digital distances, distance transform, medial axis transform, component labeling, thinning, morphological processing, extension to gray scale morphology.

**MODULE II IMAGE TRANSFORMS 9**

1D DFT, 2D transforms - DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Wavelet transform.

**MODULE III SEGMENTATION OF GRAY LEVEL IMAGES 9**

Histogram of gray level images, multilevel thresholding, Optimal thresholding using Bayesian classification, Watershed and Dam Construction algorithms for segmenting gray level image. Detection of edges and lines: First order and second order edge operators, multi-scale edge detection, Canny's edge detection algorithm, Hough transform for detecting lines and curves, edge linking.

**MODULE IV IMAGE ENHANCEMENT AND COLOR IMAGE PROCESSING 9**

Point processing, Spatial Filtering, Frequency domain filtering, multi-spectral image enhancement, image restoration. Color Representation, Laws of color matching, chromaticity diagram, color enhancement, color image segmentation, color edge detection, color demosaicing.

**MODULE V IMAGE COMPRESSION 9**

Lossy and lossless compression schemes, prediction based compression schemes, vector quantization, sub-band encoding schemes, JPEG compression standard, Fractal compression scheme, Wavelet compression scheme.

**Total: 45 HOURS**

**REFERENCES:**

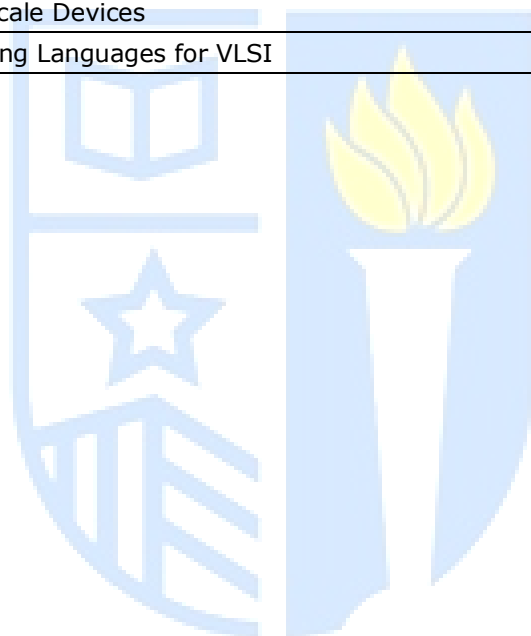
1. A.K. Jain, "Fundamentals of Digital Image Processing", Prentice-Hall, Addison-Wesley, 1989.
2. Bovik (ed.), "Handbook of Image and Video Processing", Academic Press, 2000.
3. B. Jähne, "Practical Handbook on Image Processing for Scientific Applications", CRC Press, 1997.
4. Bernd Jähne, Digital Image Processing, Springer-Verlag Berlin Heidelberg 2005.
5. Gonzalez and Woods, Digital Image Processing, Prentice-Hall.
6. J. C. Russ. The Image Processing Handbook. CRC, Boca Raton, FL, 4th edn., 2002.
7. J. S. Lim, "Two-dimensional Signal and Image Processing" Prentice-Hall, 1990.
8. . M. Petrou, P. Bosdogianni, "Image Processing, The Fundamentals", Wiley, 1999.

**Semester III**

Sl.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
<b>THEORY</b>								
1	P19VL3XX	Program Elective V	PE	3	3	0	0	3
2	P19OE4XX	Open Elective	OE	3	3	0	0	3
<b>PRACTICALS</b>								
3	P19VL202	Project Work Phase I	PW	16	0	0	16	8
<b>TOTAL</b>				<b>22</b>	<b>6</b>	<b>0</b>	<b>16</b>	<b>14</b>

**PROGRAM ELECTIVES (PE)**

Sl.No.	Course Code	Course Title	Category	L	T	P	C
1	P19VL317	MEMS and NEMS	PE	3	0	0	3
2	P19VL318	Signal Integrity for High Speed Design	PE	3	0	0	3
3	P19VL319	Nanoscale Devices	PE	3	0	0	3
4	P19VL320	Scripting Languages for VLSI	PE	3	0	0	3





		<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>P19VL317</b>	<b>MEMS AND NEMS</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

<b>Outcomes</b>				
CO1	Understand the operation of micro devices, micro systems and their applications		M1	K2
CO2	Design the micro devices, micro systems using the MEMS fabrication process.		M2	K3
CO3	Design concepts of micro sensors.		M3	K4
CO4	Design concepts of micro actuators.		M4	K4
CO5	Develop experience on micro/nano systems for photonics .		M5	K5

### **MODULE I OVERVIEW 9**

New trends in Engineering and Science: Micro and Nanoscale systems, Introduction to Design of MEMS and NEMS, MEMS and NEMS – Applications, Devices and structures. Materials for MEMS: Silicon, silicon compounds, polymers, metals.

### **MODULE II MEMS FABRICATION TECHNOLOGIES 9**

Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect-Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials

### **MODULE III MICRO SENSORS 9**

MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors- engineering mechanics behind these Microsensors. Case study: Piezo-resistive pressure sensor.

### **MODULE IV MICRO ACTUATORS 9**

Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces (Parallel plate, Torsion bar, Comb drive actuators), Micromechanical Motors and pumps. Case study: Comb drive actuators.

### **MODULE V NANOSYSTEMS AND QUANTUM MECHANICS 9**

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation and Wave function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

**Total : 45 HOURS**

#### **REFERENCES:**

1. Chang Liu, "Foundations of MEMS", Pearson education India limited, 2006.
2. Marc Madou, "Fundamentals of Microfabrication", CRC press 1997.
3. Stephen D. Senturia, "Micro system Design", Kluwer Academic Publishers, 2001
4. Sergey Edward Lyshevski, "MEMS and NEMS: Systems, Devices, and Structures" CRC Press, 2002.
5. Tai Ran Hsu, "MEMS and Microsystems Design and Manufacture" ,Tata Mcraw Hill, 2002.

		<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>P19VL318</b>	<b>SIGNAL INTEGRITY FOR HIGH SPEED DESIGN</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

<b>Outcomes</b>			
CO1	Identify sources affecting the speed of digital circuits.	M1	K2
CO2	Discuss the ways to Improve the signal transmission characteristics.	M2	K2
CO3	To identify sources affecting the speed of digital circuits.	M3	K2
CO4	To introduce methods to improve the signal transmission characteristics	M4	K2
CO5	Discuss about Clock Distribution And Clock Oscillators	M5	K2

**MODULE I SIGNAL PROPAGATION ON TRANSMISSION LINES 9**

Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic impedance, wave propagation, reflection, and bounce diagrams Reactive terminations – L, C, static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools,  $Z_0$  and  $T_d$  equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching, input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion

**MODULE II MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK 9**

Multi-conductor transmission-lines, coupling physics, per unit length parameters, Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits, S-parameters, Lossy and Lossless models

**MODULE III NON-IDEAL EFFECTS 9**

Non-ideal signal return paths – gaps, BGA fields, via transitions, Parasitic inductance and capacitance, Transmission line losses –  $R_s$ ,  $\tan\delta$ , routing parasitic, Common-mode current, differential-mode current, Connectors

**MODULE IV POWER CONSIDERATIONS AND SYSTEM DESIGN 9**

SSN/SSO, DC power bus design, layer stack up, SMT decoupling, Logic families, power consumption, and system power delivery, Logic families and speed Package types and parasitic, SPICE, IBIS models, Bit streams, PRBS and filtering functions of link-path components, Eye diagrams, jitter, inter-symbol interference Bit-error rate, Timing analysis

**MODULE V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS 9**

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

**Total : 45 HOURS**

**REFERENCES:**

1. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall PTR, 2003.
2. Eric Bogatin, Signal Integrity – Simplified, Prentice Hall PTR, 2003.
3. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993.
4. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley-Interscience, 2000.

		<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>P19VL319</b>	<b>NANOSCALE DEVICES</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

<b>Outcomes</b>				
CO1	Interpret novel MOSFET devices and understand the advantages of multi-gate devices	M1		K2
CO2	Discuss the physical insight of their functional characteristics	M2		K2
CO3	Interpret Nanowire Fets And Transistors At The Molecular Scale	M3		K2
CO4	Explain the effects of Radiation	M4		K2
CO5	Design of circuits using Multigate Devices	M5		K3

#### **MODULE I INTRODUCTION TO NOVEL MOSFETS 9**

MOSFET scaling, short channel effects - channel engineering - source/drain engineering - high k dielectric - copper interconnects - strain engineering, SOI MOSFET, multigate transistors - single gate - double gate - triple gate - surround gate, quantum effects - volume inversion - mobility - threshold voltage - inter subband scattering, multigate technology - mobility - gate stack

#### **MODULE II PHYSICS OF MULTIGATE MOS SYSTEMS 9**

MOS Electrostatics - 1D - 2D MOS Electrostatics, MOSFET Current-Voltage Characteristics - CMOS Technology - Ultimate limits, double gate MOS system - gate voltage effect - semiconductor thickness effect - asymmetry effect - oxide thickness effect - electron tunnel current - two dimensional confinement, scattering - mobility

#### **MODULE III NANOWIRE FETS AND TRANSISTORS AT THE MOLECULAR SCALE 9**

Silicon nanowire MOSFETs - Evaluation of I-V characteristics - The I-V characteristics for non-degenerate carrier statistics - The I-V characteristics for degenerate carrier statistics - Carbon nanotube - Band structure of carbon nanotube - Band structure of graphene - Physical structure of nanotube - Band structure of nanotube - Carbon nanotube FETs - Carbon nanotube MOSFETs - Schottky barrier carbon nanotube FETs - Electronic conduction in molecules - General model for ballistic nano transistors - MOSFETs with 0D, 1D, and 2D channels - Molecular transistors - Single electron charging - Single electron transistors

#### **MODULE IV RADIATION EFFECTS 9**

Radiation effects in SOI MOSFETs, total ionizing dose effects - single gate SOI - multigate devices, single event effect, scaling effects

#### **MODULE V CIRCUIT DESIGN USING MULTIGATE DEVICES 9**

Digital circuits - impact of device performance on digital circuits - leakage performance trade off - multi VT devices and circuits - SRAM design, analog circuit design - transconductance - intrinsic gain - flicker noise - self heating - band gap voltage reference - operational amplifier - comparator designs, mixed signal - successive approximation DAC, RF circuits.

**Total : 45 HOURS**

#### **REFERENCES:**

1. J P Colinge, "FINFETs and other multi-gate transistors", Springer - Series on integrated circuits and systems, 2008
2. Mark Lundstrom, Jing Guo, "Nanoscale Transistors: Device Physics, Modeling and Simulation", Springer, 2006
3. M S Lundstorm, "Fundamentals of Carrier Transport", 2nd Ed., Cambridge University Press, Cambridge UK, 2000

		<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>P19VL320</b>	<b>SCRIPTING LANGUAGES FOR VLSI</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

<b>Outcomes</b>				
CO1	Illustrate about the SCRIPTING And PERL		M1	K2
CO2	Interpret advanced PERL		M2	K2
CO3	Explain the concept of TCL phenomena		M3	K2
CO4	Interpret advanced TCL		M4	K2
CO5	Create TK and Java script		M5	K6

**MODULE I INTRODUCTION TO SCRIPTING AND PERL 9**

Characteristics of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

**MODULE II ADVANCED PERL 9**

Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

**MODULE III TCL 9**

The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

**MODULE IV ADVANCED TCL 9**

The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running un trusted code, The C interface.

**MODULE V TK AND JAVA SCRIPT 9**

Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK. JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Python. Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

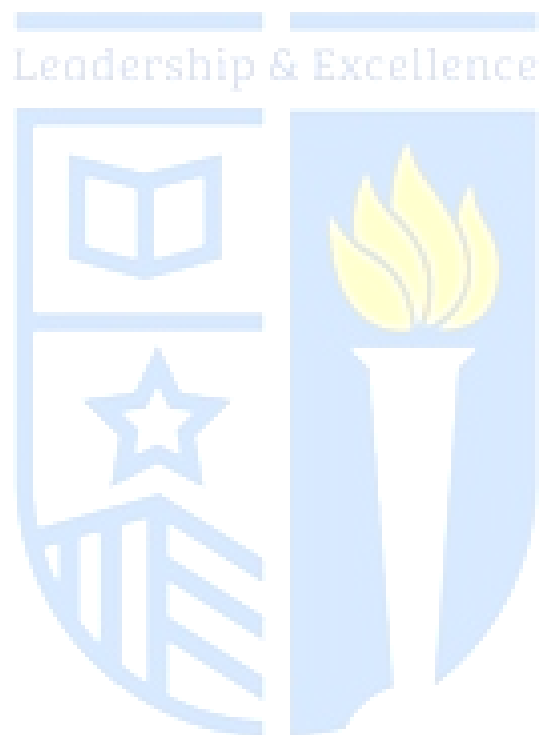
**Total : 45 HOURS**

**REFERENCES:**

1. Brent Welch, "Practical Programming in Tcl and Tk", Fourth Edition, 2003.
2. David Barron, "The World of Scripting Languages", Wiley Publications, 2000.
3. Guido van Rossum, and Fred L. Drake ", Python Tutorial, Jr., editor, Release 2.6.4
4. Randal L. Schwartz, "Learning PERL", Sixth Edition, O'Reilly.

**OPEN ELECTIVES**

<b>Sl.No.</b>	<b>Course Code</b>	<b>Course Title</b>	<b>Category</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
1	P19OE401	Business Analytics	OE	3	0	0	3
2	P19OE402	Industrial Safety	OE	3	0	0	3
3	P19OE403	Operations Research	OE	3	0	0	3
5	P19OE404	Composite Materials	OE	3	0	0	3



		<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>P190E401</b>	<b>BUSINESS ANALYTICS</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

<b>Outcomes</b>			
CO1	Identify the real world business problems and model with analytical solutions.	M1	K3
CO2	Solve analytical problem with relevant mathematics background knowledge	M2	K4
CO3	Convert any real world decision making problem to hypothesis and apply suitable statistical testing	M3	K3
CO4	Use open source frameworks for modelling and storing data.	M4	K4
CO5	Apply suitable visualization technique using R for visualizing voluminous data	M5	K3

#### **MODULE I OVERVIEW OF BUSINESS ANALYTICS 9**

Introduction – Drivers for Business Analytics – Applications of Business Analytics: Marketing and Sales, Human Resource, Healthcare, Product Design, Service Design, Customer Service and Support – Skills Required for a Business Analyst – Framework for Business Analytics Life Cycle for Business Analytics Process.

#### **MODULE II ESSENTIALS OF BUSINESS ANALYTICS 9**

Descriptive Statistics – Using Data – Types of Data – Data Distribution Metrics: Frequency, Mean, Median, Mode, Range, Variance, Standard Deviation, Percentile, Quartile, z-Score, Covariance, Correlation – Data Visualization: Tables, Charts, Line Charts, Bar and Column Chart, Bubble Chart, Heat Map – Data Dashboards.

#### **MODULE III MODELING UNCERTAINTY AND STATISTICAL INFERENCE 9**

Modeling Uncertainty: Events and Probabilities – Conditional Probability – Random Variables – Discrete Probability Distributions – Continuous Probability Distribution – Statistical Inference: Data Sampling – Selecting a Sample – Point Estimation – Sampling Distributions – Interval Estimation – Hypothesis Testing.

#### **MODULE IV ANALYTICS USING HADOOP AND MAPREDUCE FRAMEWORK 9**

Introducing Hadoop – RDBMS versus Hadoop – Hadoop Overview – HDFS (Hadoop Distributed File System) – Processing Data with Hadoop – Introduction to MapReduce – Features of MapReduce – Algorithms Using Map-Reduce: Matrix-Vector Multiplication, Relational Algebra Operations, Grouping and Aggregation – Extensions to MapReduce.

#### **MODULE V OTHER DATA ANALYTICAL FRAMEWORKS 9**

Overview of Application development Languages for Hadoop – PigLatin – Hive – Hive Query Language (HQL) – Introduction to Pentaho, JAQL – Introduction to Apache: Sqoop, Drill and Spark, Cloudera Impala – Introduction to NoSQL Databases – Hbase and MongoDB.

**Total : 45 HOURS**

#### **REFERENCES:**

1. VigneshPrajapati, "Big Data Analytics with R and Hadoop", Packt Publishing, 2013.
2. AnandRajaraman, Jeffrey David Ullman, "Mining of Massive Datasets", Cambridge University Press, 2012.
3. Jeffrey D. Camm, James J. Cochran, Michael J. Fry, Jeffrey W. Ohlmann, David R. Anderson, "Essentials of Business Analytics", Cengage Learning, second Edition, 2016
4. U. Dinesh Kumar, "Business Analytics: The Science of Data-Driven Decision Making", Wiley, 2017.
5. A. Ohri, "R for Business Analytics", Springer, 2012
6. Umesh R Hodeghatta, UmeshaNayak, "Business Analytics Using R – A Practical Approach", Apress, 2017
7. Rui Miguel Forte, "Mastering Predictive Analytics with R", Packt Publication, 2015.

		<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>P190E402</b>	<b>INDUSTRIAL SAFETY</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

<b>Outcomes</b>			
CO1	Get exposed to safety concepts and industry hazards	M1	K2
CO2	Understand the chemical hazards	M2	K2
CO3	Analyze the noise pollution using instruments	M3	K4
CO4	Analyze the hazards using different techniques	M4	K4
CO5	Apply the regulations for safety and control of hazards	M5	K3

**MODULE I INTRODUCTION 9**

Evolution of modern safety concepts – Fire prevention – Mechanical hazards – Boilers, Pressure vessels, Electrical Exposure.

**MODULE II CHEMICAL HAZARDS 9**

Chemical exposure – Toxic materials – Ionizing Radiation and Non-ionizing Radiation - Industrial Hygiene – Industrial Toxicology.

**MODULE III ENVIRONMENTAL CONTROL 9**

Industrial Health Hazards – Environmental Control – Industrial Noise - Noise measuring instruments, Control of Noise, Vibration, - Personal Protection.

**MODULE IV HAZARD ANALYSIS 9**

System Safety Analysis –Techniques – Fault Tree Analysis (FTA), Failure Modes and Effects Analysis (FMEA), HAZOP analysis and Risk Assessment

**MODULE V SAFETY REGULATIONS 9**

Explosions – Disaster management – catastrophe control, hazard control ,Safety education and training - Factories Act, Safety regulations Product safety – case studies.

**Total : 45 HOURS**

**REFERENCES:**

1. John V.Grimaldi, "Safety Management", AITB S Publishers, 2003.
2. Safety Manual, "EDEL Engineering Consultancy", 2000.
3. David L.Goetsch, "Occupational Safety and Health for Technologists", 5th Edition, Engineers and Managers, Pearson Education Ltd., 2005

		<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>P190E403</b>	<b>OPERATIONS RESEARCH</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

<b>Outcomes</b>				
CO1	Understand basics of operation research and optimization problems	M1		K2
CO2	Apply transportation and network models	M2		K3
CO3	Understand inventory control models	M3		K2
CO4	Analyze the Queueing systems and models	M4		K4
CO5	Apply decision models for optimization problems	M5		K3

**MODULE I OPERATIONS RESEARCH 10**

The phase of an operation research study – Linear programming – Graphical method– Simplex algorithm – Duality formulation – Sensitivity analysis.

**MODULE II TRANSPORTATION MODELS AND NETWORK MODELS 9**

Transportation Assignment Models –Traveling Salesman problem-Networks models – Shortest route – Minimal spanning tree – Maximum flow models –Project network – CPM and PERT networks – Critical path scheduling – Sequencing models

**MODULE III INVENTORY MODELS 8**

Inventory models – Economic order quantity models – Quantity discount models – Stochastic inventory models – Multi product models – Inventory control models in practice.

**MODULE IV QUEUEING MODELS 8**

Queueing models - Queueing systems and structures – Notation parameter – Single server and multi-server models – Poisson input – Exponential service – Constant rate service – Infinite population – Simulation.

**MODULE V DECISION MODELS 10**

Decision models – Game theory – Two person zero sum games – Graphical solution- Algebraic solution– Linear Programming solution – Replacement models – Models based on service life – Economic life– Single / Multi variability search technique – Dynamic Programming – Simple Problem.

**Total : 45 HOURS**

**REFERENCES:**

1. Hillier and Libeberman, "Operations Research", Holden Day, 2005
2. Taha H.A., "Operations Research", Sixth Edition, Prentice Hall of India, 2003.
3. Bazara M.J., Jarvis and Sherali H., "Linear Programming and Network Flows", John Wiley, 2009.
4. Budnick F.S., "Principles of Operations Research for Management", Richard D Irwin, 1990.
5. Philip D.T. and Ravindran A., "Operations Research", John Wiley, 1992.
6. Shenoy G.V. and Srivastava U.K., "Operation Research for Management", Wiley Eastern, 1994.
7. Tulsian and Pasdey V., "Quantitative Techniques", Pearson Asia, 2002.



		L	T	P	C
<b>P190E405</b>	<b>COMPOSITE MATERIALS</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

Upon completion of this course, students will be able to

Outcomes			
CO1	Summarize the various types of Fibers, Equations and manufacturing methods for Composite materials	M1	K2
CO2	Derive Flat plate Laminate equations	M2	K3
CO3	Analyze Lamina strength	M3	K4
CO4	Analyze the thermal behavior of Composite laminates	M4	K4
CO5	Analyze Laminate flat plates	M5	K3

### **MODULE I INTRODUCTION, LAMINA CONSTITUTIVE EQUATIONS & MANUFACTURING 9**

Definition –Need – General Characteristics, Applications. Fibers – Glass, Carbon, Ceramic and Aramid fibers. Matrices – Polymer, Graphite, Ceramic and Metal Matrices – Characteristics of fibers and matrices. Lamina Constitutive Equations: Lamina Assumptions – Macroscopic Viewpoint. Generalized Hooke's Law. Reduction to Homogeneous Orthotropic Lamina – Isotropic limit case, Orthotropic Stiffness matrix ( $Q_{ij}$ ), Typical Commercial material properties, Rule of Mixtures. Generally Orthotropic Lamina –Transformation Matrix, Transformed Stiffness. Manufacturing: Bag Moulding Compression Moulding – Pultrusion – Filament Winding – Other Manufacturing Processes

### **MODULE II FLAT PLATE LAMINATE CONSTITUTE EQUATIONS 9**

Definition of stress and Moment Resultants. Strain Displacement relations. Basic Assumptions of Laminated anisotropic plates. Laminate Constitutive Equations – Coupling Interactions, Balanced Laminates, Symmetric Laminates, Angle Ply Laminates, Cross Ply Laminates. Laminate Structural Moduli. Evaluation of Lamina Properties from Laminate Tests. Quasi-Isotropic Laminates. Determination of Lamina stresses within Laminates.

### **MODULE III LAMINA STRENGTH ANALYSIS 9**

Introduction - Maximum Stress and Strain Criteria. Von-Misses Yield criterion for Isotropic Materials. Generalized Hill's Criterion for Anisotropic materials. Tsai-Hill's Failure Criterion for Composites. Tensor Polynomial (Tsai-Wu) Failure criterion. Prediction of laminate Failure.

### **MODULE IV THERMAL ANALYSIS 9**

Assumption of Constant C.T.E's. Modification of Hooke's Law. Modification of Laminate Constitutive Equations. Orthotropic Lamina C.T.E's. C.T.E's for special Laminate Configurations – Unidirectional, Off-axis, Symmetric Balanced Laminates, Zero C.T.E laminates, Thermally QuasiIsotropic Laminates

### **MODULE V ANALYSIS OF LAMINATED FLAT PLATES 9**

Equilibrium Equations of Motion. Energy Formulations. Static Bending Analysis. Buckling Analysis. Free Vibrations – Natural Frequencies.

**Total : 45 HOURS**

#### **REFERENCES:**

- Gibson, R.F., "Principles of Composite Material Mechanics", Second Edition, McGraw-Hill, CRC press in progress, 1994,
- Hyer, M.W., "Stress Analysis of Fiber – Reinforced Composite Materials", McGraw Hill, 1998
- Agarwal, B.D., and Broutman L.J., "Analysis and Performance of Fiber Composites", John Wiley and Sons, New York, 1990.
- Halpin, J.C., "Primer on Composite Materials, Analysis", Technomic Publishing Co., 1984
- Issac M. Daniel and OriIshai, "Engineering Mechanics of Composite Materials", Oxford University Press- 2006, First Indian Edition - 2007
- Mallick, P.K., Fiber, "Reinforced Composites: Materials, Manufacturing and Design", Maneel Dekker Inc, 1993.

**Semester IV**

Sl.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
<b>PRACTICALS</b>								
1	P19VL203	Project Work Phase II	PW	32	0	0	32	16
<b>TOTAL</b>				<b>32</b>	<b>0</b>	<b>0</b>	<b>32</b>	<b>16</b>

