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Department of Electronics and Communication Engineering

Inviting the students and Staff to join The One Day Webinar on

"Challenges and Opportunities in VLSI Design"

Dr.S.Dhanasekar

Asso. Prof., Department of ECE
Sri Eshwar College of Engineering, Coimbatore.

JUNE
12

11.00 AM to 12.30 PM

Patron
Dr.K.S. Saji
Principal

Convenor
Dr.A.S. Radhamani
Professor/Head

Coordinator
Mr. V. Somasundaram
AP/ECE

Organizing Committe

Dr. E. Praynlin AP/ECE, Mrs. J.L. Jini Mary, AP/ECE, Ms. M. Augusta Angel, AP/ECE

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Meeting Number : 1668613680, Password - vlsi@123

Dr.Dhanasekar Subramaniyam <dhanasekarsubramaniyam@sece.ac.in>

Webinar resource person - reg

Dr.Dhanasekar Subramaniyam <dhanasekarsubramaniyam@sece.ac.in> Mon, June 8, 2020 at 10:12 AM
To: HOD Electronics and Communication <hodece@vvcoe.org>

Dear Mr. Somasundaram,
I am very happy to see your email, and you can consider this email as a confirmation for handling a session on 12.06.2020

Thanks and Regards,
Dr.S.DHANASEKAR,
Associate Professor,
Department of ECE,
Sri Eshwar College of Engineering,
Coimbatore.
Mobile No: 8760464534

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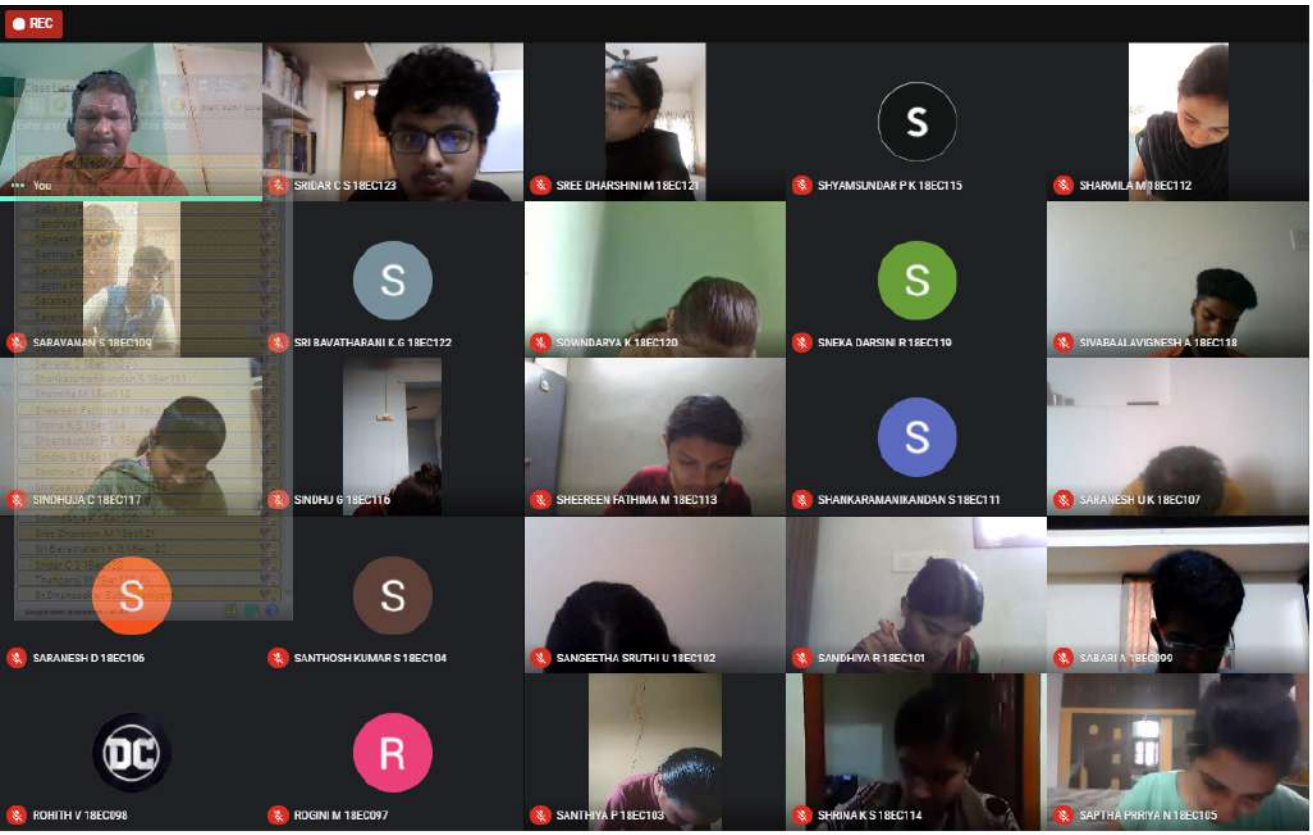
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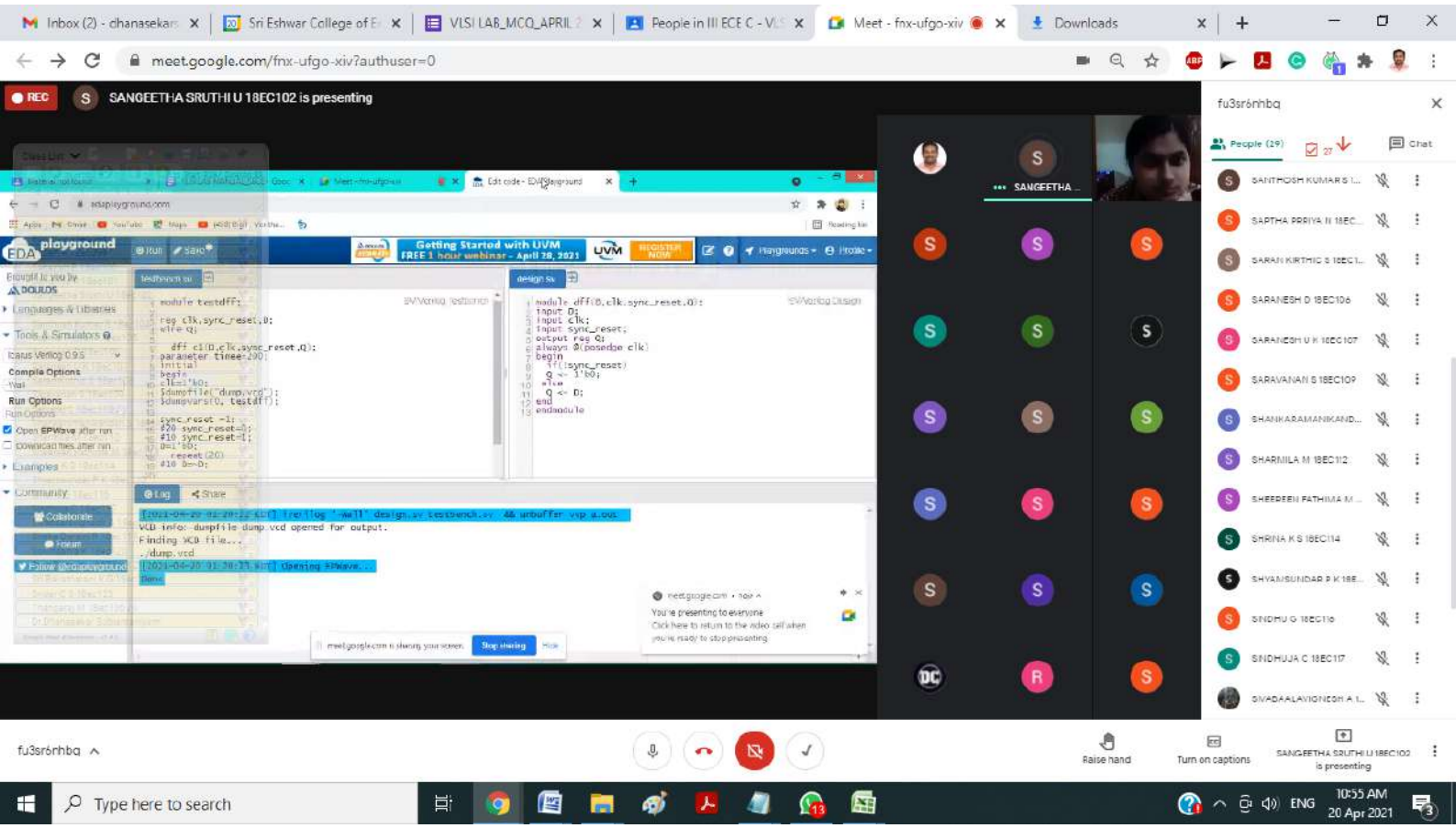
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testbench.sv
design.sv
module testdff;
reg clk,sync_reset,D;
wire Q;
dff c1(D,clk,sync_reset,Q);
parameter time=200;
initial
begin
clk=1'b0;
$dumpfile("dump.vcd");
$dumpvars(0, testdff);
sync_reset =1;
#20 sync_reset=0;
#10 sync_reset=1;
D=1'b0;
repeat(20)
#10 D=~D;
module dff(D,clk,sync_reset,Q);
input D;
input clk;
input sync_reset;
output reg Q;
always @(posedge clk)
begin
if(!sync_reset)
Q <= 1'b0;
else
Q <= D;
end
endmodule
Log
Share
VCD info: dumpfile dump.vcd opened for output.
Finding VCD file...
./dump.vcd
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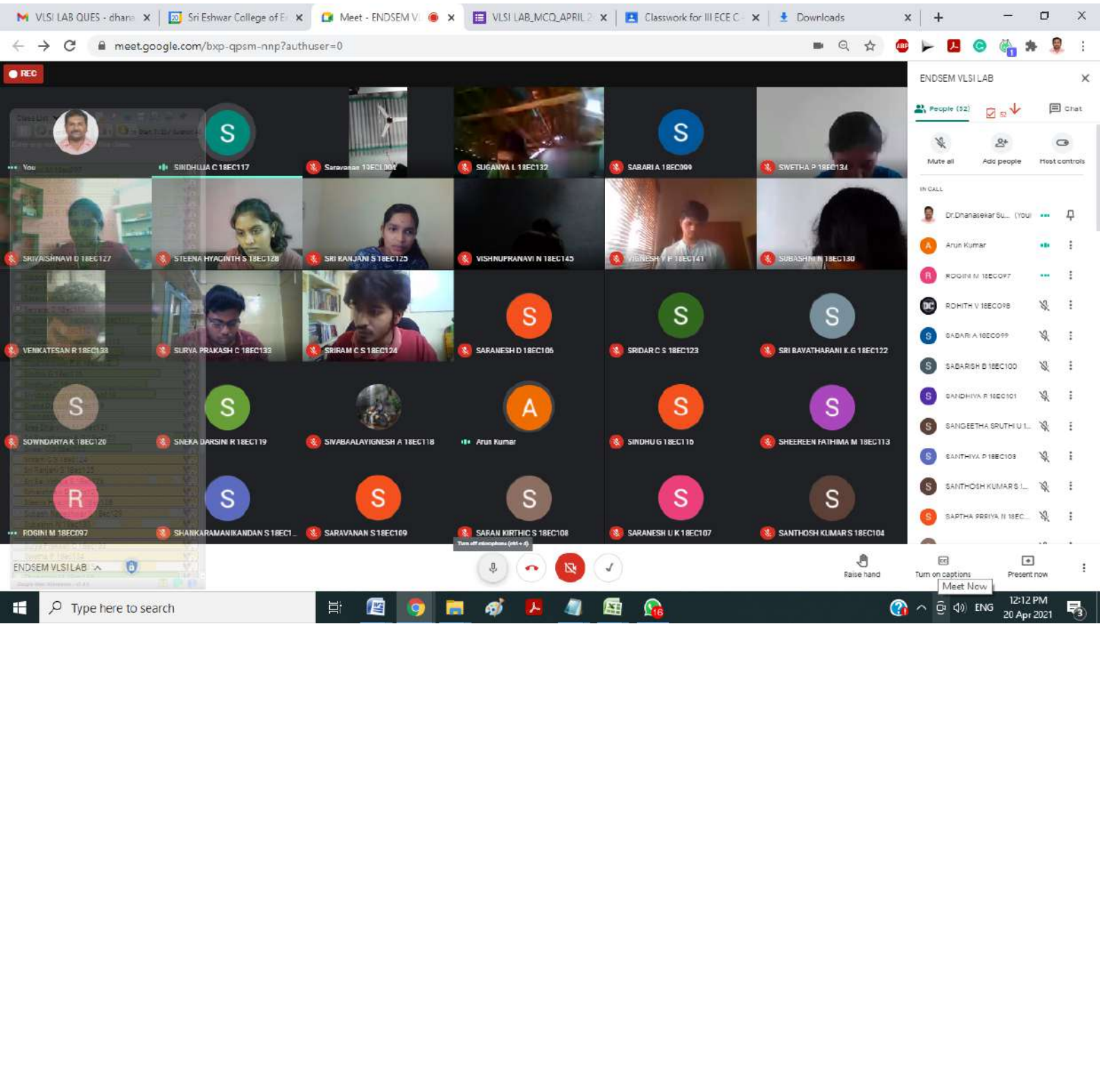
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V V COLLEGE OF ENGINEERING

(Approved by AICTE and affiliated to Anna University - Chennai)

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22.06.2020

TO WHOMSOEVER IT MAY CONCERN

This is to certify that Dr. S. Dhanasekar, Associate Professor, Department of Electronics and Communication Engineering, Sri Eshwar College of Engineering, Coimbatore delivered a lecture in an one day webinar on "Challenges and Opportunities in VLSI Design" conducted by V V College of Engineering to the participants from various colleges on 12.06.2020. Around 150 participants attended the webinar. The lecture was very useful and inspired them.

Principal

Dr. K.S. SAJI, M.E., Ph.D.,
Principal,
V V College of Engineering,
V V Nagar, Arasoor Sathankulam Tk.,
Tuticorin Dist., Tamilnadu, Pin - 628 656.

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